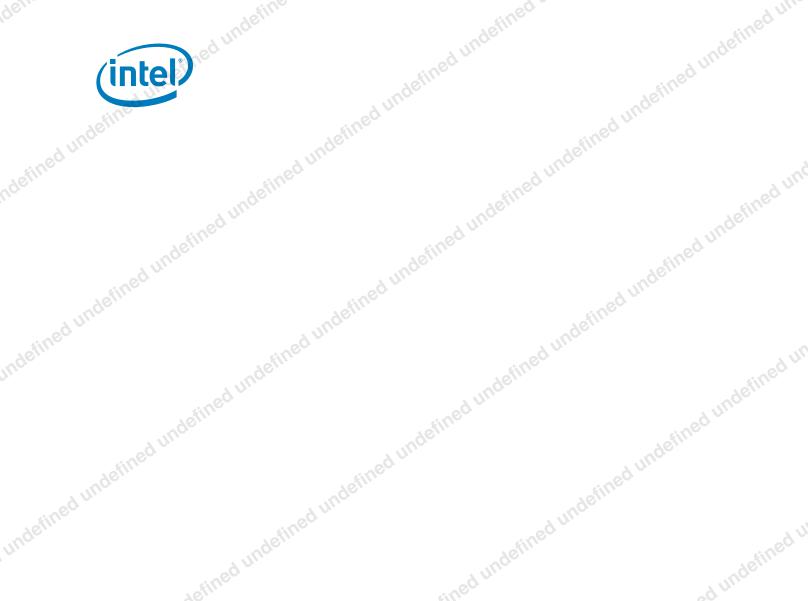


6th Generation Intel® Proc Families for S-Plate **Processor**

July 2020 Desk Desk undefined undefi

undefined undefi



You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting: http://www.intel.com/design/literature.htm.

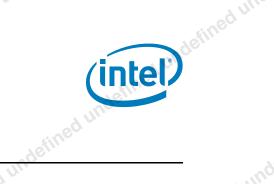
Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at [most relevant URL to your product].

No computer system can be absolutely secure.

cher country in the state of th y of oth ved. Intel, Intel Core, Celeron, Pentium, Xeon, and the Intel logo are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

ined undefined Datasheet, Volume 1 of 2

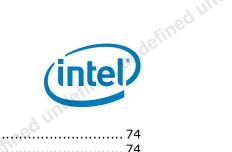


		The day	defined u
Intro	duction	defined un	ed u
1.1		ted Technologies	file
1.1	1.1.1	Operating System Support	
1.2	7777	Management Support	
1,2	1.2.1	Processor Core Power Management	
401.	1.2.2	System Power Management	
	1.2.3	Memory Controller Power Management	
	1.2.4	Processor Graphics Power Management	
		1.2.4.1 Memory Power Savings Technologies	
		1.2.4.2 Display Power Savings Technologies	
		1.2.4.3 Graphics Core Power Savings Technologies	
1.3	Therma	ıl Management Support14	
1.4		e Support	
1.5	Process	or Testability	16/11/
1.6		ology 15	
1.7	Related	Documents	
Total			
	C	Mamanu Interfere	
2.1	-	Memory Interface	
7.	2.1.1	System Memory Technology Supported	
		2.1.1.1 DDR3L/-RS Supported Memory Modules and Devices	
	212		
	2.1.2	System Memory Timing Support	
	2.1.3	System Memory Organization Modes	
	2.1.4	System Memory Frequency	
	2.1.5	Technology Enhancements of Intel [®] Fast Memory Access	46/11
	2.1.6	Data Scrambling	ino
	2.1.7	DDR I/O Interleaving	
	2.1.8	Data Swapping	
90	2.1.9	DRAM Clock Generation	
		DRAM Reference Voltage Generation	
2.2		press* Graphics Interface (PEG)	
	2.2.1	PCI Express* Support	
	2.2.2	PCI Express* Architecture	
	2.2.3	PCI Express* Configuration Mechanism	
	2.2.4	PCI Express* Equalization Methodology	
2.3		Media Interface (DMI)	define
	2.3.1	DMI Error Flow	46/11
- 4	2.3.2	DMI Link Down	100
2.4		or Graphics	
	2.4.1	API Support (Windows*)	
~9,	2.4.2	Media Support (Intel® QuickSync & Clear Video Technology HD)	
efined		2.4.2.1 Hardware Accelerated Video Decode	
		2.4.2.3 Hardware Accelerated Video Processing	
		2.4.2.4 Hardware Accelerated Transcoding	
	2.4.3		
	2.4.4	Camera Pipe Support	
	2.4.5	GEN 9 Video Analytics	
		GEN 9 (Generation 9) Block Diagram	
	2.4.7	GEN 9 (Generation 9) Block Diagram	Yeji.
	4.T./	or 2 or apriles i requeries	1100
	46jii		
	1100	YEJ,	
asheet Vol	ume 1 of 2	The state of the s	
	U.IIC 1 01 Z	ed to	
define			
		de.	
		7 1/1, Jan 19 19 19 19 19 19 19 19 19 19 19 19 19	
		The Authority of the Au	

indefined undefined undefineu



		define	sined.		ed u
	5.	Interfaces	, Inder		Jundefined u
/inte				od	June
			ndein	4efine	
Sine		ned "		4 unos	
2.5	Display	Interfaces DisplayPort*			.36
inced to	2.5.1 2.5.2	High-Definition Multimedia I			.+0
	2.5.3	Digital Video Interface (DVI))		.41
	2.5.4 2.5.5	embedded DisplayPort* (eD Integrated Audio			
	2.5.6	Multiple Display Configuration	ons (Dual Channel DDR) .		.42
	2.5.7	Multiple Display Configuration			
	2.5.8 2.5.9	High-Bandwidth Digital Cont Display Link Data Rate Supp			
ed	2.5.10	Display Bit Per Pixel (BPP) S	Support		.44
defill.		Display Resolution per Link			
2.6	2.6.1	n Environmental Control Inte PECI Bus Architecture			
eine 3 Tec	_				
3.1	Intel®	s Virtualization Technology (Int	tel [®] VT)	<u> </u>	.48
	3.1.1	Intel [®] Virtualization Technol Architecture (Intel [®] VT-X)	logy (Intel $^{ m ext{ iny P}}$ VT) for IA-32	2, Intel [®] 64 and Intel [®]	10 Fine
	3.1.2	Intel® Virtualization Technol	logy (Intel® VT) for Direc	ted I/O (Intel [®] VT-d)	.50
3.2	Securit	Intel [®] Virtualization Technoly y Technologies			.53
4	3.2.1	Intel® Trusted Execution Te	chnology (Intel® TXT)	on (Intal® AEC NI)	.53
	3.2.2 3.2.3	Intel [®] Advanced Encryption PCLMULQDQ (Perform Carry			
deili	3.2.4	Intel® Secure Key			.54
dulle	3.2.5	Execute Disable Bit			
	3.2.6 3.2.7	Boot Guard Technology Supervisor Mode Execution			
	3.2.8	Intel Supervisor Mode Acces	ss Protection (SMAP)		.55
	3.2.9	Intel [®] Memory Protection Ex Intel [®] Software Guard Exter	xtensions (Intel [®] MPX)		.55
	3.2.10	Intel® Virtualization Technol	logy (Intel® VT) for Direc	:ted I/O (Intel [®] VT-d)	.56
3.3	Power	and Performance Technologie	es		.57
	3.3.1 3.3.2	Intel [®] Hyper-Threading Tecl Intel [®] Turbo Boost Technolo	hnology (Intel® HT Techn ogy 2.0	ology)	.57 57
	3.3.2	3.3.2.1 Intel [®] Turbo Boost	t Technology 2.0 Frequen	cy	.57
	3.3.3	Intel® Advanced Vector Exte	ensions 2 (Intel [®] AVX2)		.58
ed un	3.3.4 3.3.5	Intel [®] 64 Architecture x2AP Power Aware Interrupt Rout	IC ing (PAIR)		.58 59
efine	3.3.6	Intel® Transactional Synchro	onization Extensions (Inte	el® TSX-NI)	.59
defined undefined		Image Signal Processor (Inte	el [®] ISP)	<u> </u>	.60
3.5	3.4.1 Debua	Platform Imaging Infrastruct	ture		.60 .61
	3.5.1	Intel [®] Processor Trace			.61
4 Pov		gement			
4.1		ed Configuration and Power			
4.2		sor IA Core Power Manageme OS/HW controlled P-states			
Inoc		4.2.1.1 Enhanced Intel® S	${\sf SpeedStep}^{ exttt{ iny B}}$ ${\sf Technology} \dots$.66
inced of	4.2.2	4.2.1.2 Intel [®] Speed Shift Low-Power Idle States			
defill	4.2.3	Requesting Low-Power Idle			.68
U.	4.2.4	Processor IA core C-State R	ules	(/-	.68
	4.2.5 4.2.6	Package C-States Package C-States and Displa			. /0 . 73
	7.2.0	Tackage C-States and Displa	ay inconditions		.68 .68 .70 .73
4 4 stined undefin	ed nue	Package C-States and Displa	, muge,	Datasheet, Volume 1	of 2
ight		2.4			
Inde		defil		fine	
ined to		Aune		inde.	
16/11.				900	



	defin sines	
defined undefined unde	efined undefined undefined undefined (intel) defined	
AG	(intel)	
ed unc	inder	
iefinee	ined L.	
4.3	Integrated Memory Controller (IMC) Power Management	
	4.3.2 DRAM Power Management and Initialization	
	4.3.2.1 Initialization Role of CKE	I III.
	4.3.2.3 Dynamic Power-Down	
	4.3.3 DDR Electrical Power Gating (EPG)77	
4.4	4.3.4 Power Training	
4.5 4.6	Direct Media Interface (DMI) Power Management	
adeliii 4.0	4.6.1 Memory Power Savings Technologies	
ed m.	$4.6.1.1$ Intel $^{\otimes}$ Rapid Memory Power Management (Intel $^{\otimes}$ RMPM)	
define	4.6.2 Display Power Savings Technologies	711
	4.6.2.1 Intel [®] (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port	
	4.6.2.2 Intel [®] Automatic Display Brightness	
	4.6.2.4 Intel [®] Display Power Saving Technology (Intel [®] DPST) 6.0	
4 un	4.6.2.5 Low-Power Single Pipe (LPSP)	
Stines	4.6.3.1 Intel [®] Graphics Dynamic Frequency	
"Inge"	4.6.3.3 Dynamic FPS (DFPS)	
4.7	Voltage Optimization	
5 Therr 5.1	mal Management	-d 0
71.	5.1.1 Thermal Considerations	
	5.1.2 Intel [®] Turbo Boost Technology 2.0 Power Monitoring	
	5.1.3.1 Package Power Control 82 5.1.3.2 Platform Power Control 83	
ned th	5.1.3.3 Turbo Time Parameter (Tau)	
defill	5.1.4 Configurable TDP (cTDP) and Low-Power Mode	
undefined undefined u	5.1.4.2 Low-Power Mode	
elinee	5.1.5.1 Adaptive Thermal Monitor	
	5.1.5.2 Digital Thermal Sensor	eq.
	5.1.5.4 Bi-Directional PROCHOT#	
	5.1.5.6 Thermal Solution Design and PROCHOT# Behavior	
21	5.1.5.7 Low-Power States and PROCHOT# Behavior	
	5.1.5.9 Critical Temperature Detection	
inder	5.1.5.11 MSR Based On-Demand Mode	
ined v.	5.1.6 Intel® Memory Thermal Management	
undefined undefined v	5.1.7 Scenario Design Power (SDP)	A
J. U	5.2.1 Thermal Profile for PCG 2015D Processor	Wen
	5.2.2 Thermal Profile for PCG 2015C Processor	
	nder.	
Datasheet, Volu	5.1.6 Inter Memory Thermal Management	
Datasheet, Volu	sineo al unit	
dunc	inder.	
fines	ned to	



		adefine		ined	ined.
(in	tol [®]	Jundefine	undefined undef		efined undefined
(III	IEI		indefill	۸	elinee
Gine				d uno	
ned undefin.	5.2.3 5.2.4	Thermal Profile for PCG 20 Thermal Profile for PCG 20	15B Processor		9/
	5.2.5	Thermal Metrology			99
6 S		ription			
0.		n Memory Interface press* Graphics (PEG) Signa			
	.3 Direct	Media Interface (DMI) Signa	ıls		104
		and Miscellaneous Signals ded DisplayPort* (eDP*) Sig			
	.6 Display	/ Interface Signals			106
		sor Clocking Signalsility Signals			
	.9 Error a	nd Thermal Protection Signa	als		108
		Sequencing Signalssor Power Rails			109 110
6.	.12 Ground	d, Reserved and Non-Critical	to Function (NCTF)	Signals	111
		sor Internal Pull-Up/Pull-Dov			
	.1 Process	ecificationssor Power Rails			112
	7.1.1	Power and Ground Pins			112
. 7	7.1.2 .2 DC Spe	V _{CC} Voltage Identification (ecifications	(VID)		112 113
ined undefir?	7.2.1	Processor Power Rails DC S	Specifications		113
d unc.		7.2.1.1 Vcc DC Specificat 7.2.1.2 Vcc _{GT} DC Specific			
inec		7.2.1.3 VDDQ DC Specifi	cations		116
,*		7.2.1.4 VccSA DC Specifi 7.2.1.5 VccIO DC Specifi	cations		117
		7.2.1.6 VccST DC Specifi 7.2.1.7 VccPLL DC Specif			
	7.2.2	Processor Interfaces DC Sp	ecifications		119
	Inge	7.2.2.1 DDR3L/-RS DC S 7.2.2.2 DDR4 DC Specific	cations		120
				ecifications Decifications	
		7.2.2.5 embedded Displa	yPort* (eDP*) DC S	Specification	122
od um		7.2.2.6 CMOS DC Specifi 7.2.2.7 GTL and OD DC S	cations Specifications		123 123
		7.2.2.8 PECI DC Characte	eristics		124
efined undefin	ackage Me	chanical Specifications			125
		ge Mechanical Attributes ge Storage Specifications			125
9 P	rocessor La	and Information			
Figur	es	or Line Platforms	ed une		
1-1	S-Processo	or Line Platforms	L DOW		12
1-2 2-1		DP Connector for Processor a			
2-2	Interleave	(IL) and Non-Interleave (NI	IL) Modes Mapping .		25
2-3 2-4		ss* Related Register Structu lytics Common Use Cases			
2-5	GEN 9 Bloo	ck Diagram		<u>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</u>	35
2-6	Processor	Display Architecture (with 3	DDI Ports as an Ex	ample)	39
6 Garage	, unde		DDI FOILS d'S dII EX		efine
6			ad un	Datasheet, V	olume 1 of 2
	1		Inc	ined	
ed m.		unde		adefii.	
lefine				ed un	



		define ad
		DisplayPort* Overview
		ndefined und (intel) de l'intel
		der (Intel)
	eg u	, uno
16/11/	2.7	and the state of t
unois	2-7 2-8	HDMI* Overview
	2-9	Example for PECI Host-Clients Connection
	2-10	Example for PECI EC Connection
	3-1 3-2	Device to Domain Mapping Structures
	3-3	Platform Imaging Infrastructure
	4-1 4-2	Processor Power States
	4-2	Idle Power Management Breakdown of the Processor IA Cores
	4-4	Package C-State Entry and Exit71
defi		Package Power Control
4 Une		Thermal Test Vehicle Thermal Profile for PCG 2015D Processor
	5-4	Thermal Test Vehicle Thermal Profile for PCG 2015B Processor
e,		Thermal Test Vehicle Thermal Profile for PCG 2015A Processor
		Input Device Hysteresis
		Land Map (Top View, Upper-Left Quadrant)
		Land Map (Top View, Upper-Right Quadrant)
		ed m.
de		Lefine inco
og m. I	ables	S Processor Lines
Silve	1-1 1-2	Terminology
	1-3	Related Documents
		Processor DRAM Support Matrix
		Supported DDR3L/-RS Non-ECC SODIMM Module Configurations (S-Processor Line)20
	2-4	Supported DDR4 Non-ECC UDIMM Module Configurations (S-Processor Line)21
		Supported DDR4 Non-ECC SODIMM Module Configurations (S-Processor Line)
		Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping
Indi		PCI Express* Bifurcation and Lane Reversal Mapping
		PCI Express* Maximum Transfer Rates and Theoretical Bandwidth
4efill.	2-11	Hardware Accelerated Video Encode
ndefined und		Switchable/Hybrid Graphics Support
		GT2 Graphics Frequency (S-Processor Line)
	2-15	embedded DisplayPort* (eDP*)/DDI Ports Availability
		Display Technologies Support
		Processor Supported Audio Formats over HDMI* and DisplayPort*
	2-19	Display Resolution
4 Une		S-Processor Line Display Resolution Configuration
	2-22	
agen.	2-23	Display Link Data Rate Support
Indefined un		Display Resolution and Link Rate Support
	2-26	Supported Resolutions1 for HBR2 (5.4Gbps) by Link Width
		defin.
=		HDCP Display supported Implications
Da Lefined un	tasheet,	Volume 1 of 2 7
	96,	Aefine and the second of the s
ed ui		i mo.
efine		ingo and unit



		e ined undefined undefined undefined of unit	Jefined undefin	ed ul
		d nug	defil	
	/:-	Pec ed u.	4 Unos	
	(UNU	er	eineo,	
	-	d und	'el	
26		Supported Resolutions1 for HBR (2.7Gbps) by Link Width	45	
, uno	2-27 4-1	System StatesSystem States	45	
	4-2	Processor IA Core/Package State Support	65	
	4-3	Integrated Memory Controller (IMC) States		20
	4-4 4-5	PCI Express* Link States		
	4-6	G, S, and C Interface State Combinations		
	4-7	Deepest Package C-State Available	73	
	4-8 5-1	Targeted Memory State Conditions		
	5-1 5-2	Configurable TDP Modes		
	5-3	Low Power and TTV Specifications (S-Processor Line)		
inc	5-4	Thermal Test Vehicle Thermal Profile for PCG 2015D Processor		
	5-5 5-6	Thermal Test Vehicle Thermal Profile for PCG 2015C Processor		
	5-7	Thermal Test Vehicle Thermal Profile for PCG 2015A Processor		
	6-1	Signal Tables Terminology	100	
	6-2	DDR3L/-RS Memory Interface	101	
	6-3 6-4	DDR4 Memory Interface	102	
	6-5	DMI Interface Signals		
	6-6	Reset and Miscellaneous Signals	105	
	6-7	embedded DisplayPort* Signals		
	6-8 6-9	Display Interface Signals		
9 011		Testability Signals		
		Error and Thermal Protection Signals		
		Processor Power Pails Signals		
		Processor Power Rails Signals		"EIVE
		Processor Internal Pull-Up/Pull-Down Terminations		
	7-1	Processor Power Rails		
	7-2 7-3	Processor IA Core (Vcc) Active and Idle Mode DC Voltage and Current Specification Processor Graphics (Vcc _{GT}) Supply DC Voltage and Current Specifications		
	7-3 7-4	Memory Controller (VDDQ) Supply DC Voltage and Current Specifications		
	7-5	System Agent (VccSA) Supply DC Voltage and Current Specifications	117	
. 0	7-6	Processor I/O (Vcc _{IO}) Supply DC Voltage and Current Specifications		
ineo.	7-7 7-8	Vcc Sustain (VccST) Supply DC Voltage and Current Specifications		
defined u	7-9	Processor PLL (VccPLL) Supply DC Voltage and Current Specifications		
	7-10	Processor PLL OC (VccPLL_OC) Supply DC Voltage and Current Specifications	119	a n
		DDR3L/-RS Signal Group DC Specifications		16,11
		DDR4 Signal Group DC Specifications		
	7-14	Digital Display Interface Group DC Specifications (DP*/HDMI*)	122	
		embedded DisplayPort* (eDP*) Group DC Specifications		
		CMOS Signal Group DC SpecificationsGTL Signal Group and Open Drain Signal Group DC Specifications		
		PECI DC Electrical Limits		
od'	8-1	Package Mechanical Attributes	125	
efine	8-2	Package Storage Specifications	126	
	9-1	Processor Land List	132	
ndefined '		d nur	120 132	10/11/
		inec ad m.	711.	
		der.		
	_	d nue	48111	
8	8	Datasheet, V	/olume 1 of 2	
	gei	Stille		
	ni.	inde.		
FILLER		Processor Land List		



	indefine	defin	ed	tined un
	undefined	undefined une	(inl	tel
ined undefine	evision Hist	ory	undefined une	
	adefine	illo.	ned b	ed u
Revi:		Description	Revisi	on Date
00	Initial release	ined	Augu	st 2015
00	 Addition of Intel® Pentium® p 		100	er 2015
ined und		RS Signal Group DC Specifications RS Signal Group DC Specifications	Octob	er 2015
defined undefined	 Removed references to GT3, 6 Removed references to DDR_ Table 1-1, "Processor Lines". I Section 1.5, "Processor Testal Section 2.1, "System Memory bandwidth. Table 2-4, "Supported DDR4 I Table 2-5, "Supported DDR4 I Section 2.5, "Display Interface for Multi-Stream Transport ca Section 2.5.7, "Multiple Display Section 2.5.8, "High-Bandwid Display supported Implication Section 3.3.2.1, "Intel® Turboulet. Section 3.3.2.1, "Intel® Advance Section 42.4, "Processor IA Package C-State above C8. Table 5-2, "TDP Specifications Table 5-3, "Low Power and TT Table 6-2, "DDR3L/-RS Memo Table 6-3, "DDR4 Memory Int Table 6-14, "Processor Power Table 7-2, "Processor IA core Specifications". Updated table Table 7-3, "Processor Graphic Specifications". Updated table Table 7-4, "Memory Controller Updated table Table 7-7, "Vcc Sustain (Vccs" Table 7-8, "Vcc Sustain Gated Updated table Table 7-9, "Processor PLL (Vccs") 	GT4, Vcc _{GTX} , ECC, and On-Package Cach. RCOMP[2:0] signals from Chapter 6, "Signals from Chapte	al maximum memory Updated table "." Updated table ns and Link Bandwidth Added section. ded Table 2-24, "HDCP sted section, added Updated section. remove references to dated table. May May May Current ge and Current t Specifications". Cations". Updated table nt Specifications".	2016 d Undefined
d ujides	 Updated table Table 7-12, "DDR4 Signal Gro Table 7-5, "embedded Display Table 7-18, "PECI DC Electrical 		Updated table	defines
silveo 00	: ,	_and Information I embedded DisplayPort* (eDP*) Bifurcat		ry 2017
ndeil. 00		ded DisplayPort* (eDP*)/DDI Ports Availa		st 2017
Datasi	neet, Volume 1 of 2	i Undefined un		st 2017 9
unde	Hills	adefined	indefined ut	7.7
ofineo		ed m.	ed unoe	



6//		define		raed un
		Plantefined undefined undefined undefined	undefined un	defill
	(Int	e indefine	defined	
ò	efine	stined by	und	
efined und	Revision Number	Description • Permayed Section 2.4.1 "Operating Systems Support"	Revision Date	
efille	007	Added Section 1.1.1 "Operating Systems Support" Undated Section 1.1.1 "Operating Systems Support"	May 2018	du
	009	Updated Chapter 7, Electrical Specifications Section 7.1.2 VCC Voltage Identification (VID)	July 2020	defined
		S S ined by	ed u	
	od'	Though it is the state of the s	define	
	define	fined	durie	
ed un		defilis defilis		
efille		ined in.		- 8
		d unde indefin		refinen
		defined by	6	
	6	Those index.	define	
	define		ed nue	
ed u		under		
define		ined III.		
		d unde indefin		definer
		defined by	60	nuc.
		4 under	define	
			ed une	
ed!		defi		
define		• Removed Section 2.4.1 "Operating Systems Support" • Added Section 1.1.1 "Operating Systems Support" • Updated Section 1.1.1 "Operating Systems Support" • Updated Chapter 7, Electrical Specifications Section 7.1.2 VCC Voltage Identification (VID) § §		
, ,		d nuge		define
		definer.		Junas
		d nuo	define	
			100	



10 Indefined undefined und



Introduction

The 6th Generation Intel[®] Core[™] processor, Intel[®] Pentium[®] processor, and Intel[®] Celeron[®] processor families for the Desktop S-Platform are a 64-bit, multi-core processor built on 14-nanometer process technology.

The Desktop S-Processor Lines are offered in a 2-Chip Platform and are connected to a discrete Intel® 100 Series Chipset Family Platform Controller Hub (PCH) chip on the motherboard. See the following figure.

This document covers the S-Processor Lines for Desktop (DT

Table 1-1. Processor Lines

			×					
Tille	Processor Line ¹	Package	SKU Name	Base TDP	Processor IA Cores	Graphics Configuration	On Package Cache	Platform Type
	4efill.		SKL-S 65W	54W	2	GT1		69
	und		SKL-S 35, 65W	35W, 51W	2	GT2	N/A	Silve
	S-Processor Line (DT)	LGA1151	SKL-S 35, 65W	35W, 51W	2	GT2		2-Chip
	efill		SKL-S 35, 65, 95W	35W, 65W, 91W	4	GT2	N/A	
adefined u.	S-Pentium [®] /Celeron [®] Processor Line (DT)	LGA1151	SKL-S 65W	54W	2	GT1	N/A	2-Chip
under.	Notes: 1. Processor Lines of	fering may ch	ange.			fined	1	1
	<u> </u>				20/2		•	_

Notes:

Throughout this document, the 6th Generation Intel[®] Core[™] processor, Intel[®] Pentium® processor, and Intel® Celeron® processor families may be referred to simply as "processor".

Throughout this document, the Intel® 100 Series Chipset Family Platform Controller Hub (PCH) may be referred to simply as "PCH".

This document is for the following S-Processor Line SKUs:

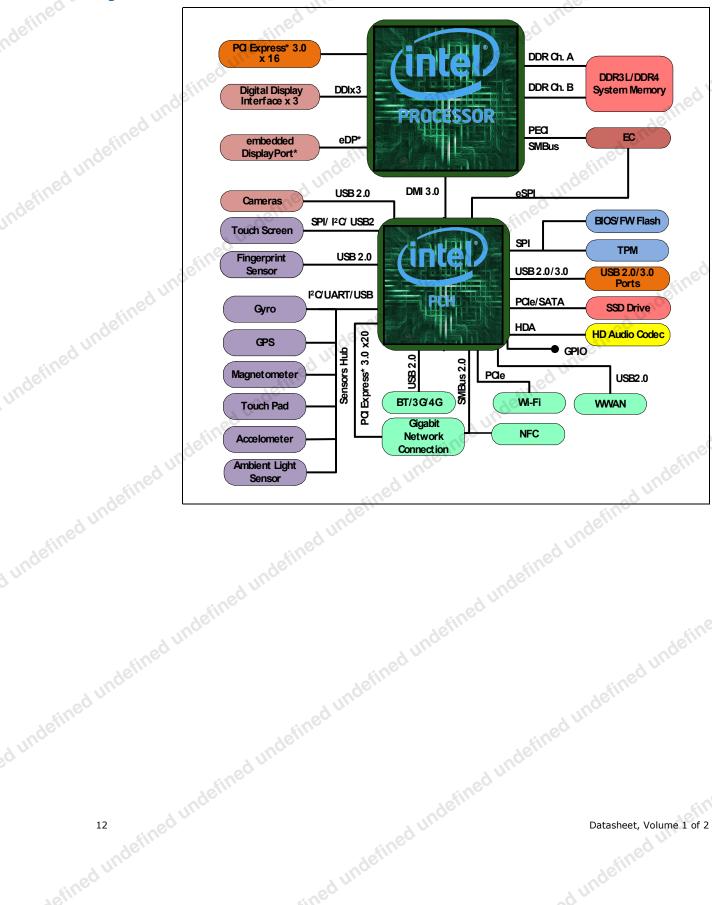
- 6th Generation Intel® Core™ processor family S-Processors
 - i7-6700K, i5-6600K, i7-6700, i5-6500, i5-6400, i7-6700T, i5-6600T, i5-6500T, i5-6400T, i3-6320, i3-6300, i3-6100, i3-6300T, i3-6100T
- Intel[®] Pentium[®] processor family S-Processors
 - G4520, G4500, G4400, G4500T, G4400T
- Intel[®] Celeron[®] processor family S-Processors
 - G3920, G3900, G3900T

Not all processor interfaces and features are present in all SKUs. For details, refer to the Specification Update.

Processor Lines offering may change.



Figure 1-1. **S-Processor Line Platforms**





1.1 Supported Technologies

- Intel[®] Virtualization Technology (Intel[®] VT)
- Intel[®] Active Management Technology 11.0 (Intel[®] AMT 11.0)
- Intel[®] Trusted Execution Technology (Intel[®] TXT)
- Intel[®] Streaming SIMD Extensions 4.2 (Intel[®] SSE4.2)
- Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel[®] Turbo Boost Technology 2.0
- Intel[®] Advanced Vector Extensions 2 (Intel[®] AVX2)
- Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)
- PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction
- Intel[®] Secure Key
- Intel® Transactional Synchronization Extensions (Intel® TSX-NI)
- PAIR Power Aware Interrupt Routing
- SMEP Supervisor Mode Execution Protection
- Intel[®] Boot Guard
- Intel[®] Software Guard Extensions (Intel[®] SGX)
- Intel® Memory Protection Extensions (Intel® MPX)
- Intel[®] Image Signal Processor (Intel[®] ISP)
- Intel® Processor Trace

Note: The availability of the features may vary between processor SKUs.

Refer to Chapter 3 for more information.

1.1.1 Operating System Support

Processor	Windows* 10	Windows* 8.1	Windows* 7	os x	Linux*	Chrome*
Line	64-bit	64-bit	64- & 32-bit		OS	OS
S-Processor Line	Yes	Yes	Yes	Yes	Yes	No

1.2 Power Management Support

1.2.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states:
 - C0, C1, C1E, C3, C6, C7, C8
- Enhanced Intel SpeedStep[®] Technology

Refer to Section 4.2 for more information.



1.2.2 System Power Management

• S0/S0ix, S3, S4, S5

Refer to Chapter 4, "Power Management" for more information.

1.2.3 Memory Controller Power Management

- Disabling Unused System Memory Outputs
- DRAM Power Management and Initialization
- Initialization Role of CKE
- Conditional Self-Refresh
- Dynamic Power Down
- DRAM I/O Power Management
- DDR Electrical Power Gating (EPG)
- Power training

Refer to Section 4.3 for more information.

1.2.4 Processor Graphics Power Management

1.2.4.1 Memory Power Savings Technologies

- Intel[®] Rapid Memory Power Management (Intel[®] RMPM)
- Intel® Smart 2D Display Technology (Intel® S2DDT)

1.2.4.2 Display Power Savings Technologies

- Intel[®] (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* port
- Intel[®] Automatic Display Brightness
- Smooth Brightness
- Intel[®] Display Power Saving Technology (Intel[®] DPST 6)
- Low Power Single Pipe (LPSP)

1.2.4.3 Graphics Core Power Savings Technologies

- Intel[®] Graphics Dynamic Frequency
- Intel[®] Graphics Render Standby Technology (Intel[®] GRST)
- Dynamic FPS (Intel® DFPS)

Refer to Section 4.6 for more information.

1.3 Thermal Management Support

- Digital Thermal Sensor
- Intel® Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)



- · Render Thermal Throttling
- · Fan speed control with DTS
- Intel® Turbo Boost Technology 2.0 Power Control

Refer to Chapter 5, "Thermal Management" for more information.

1.4 Package Support

The processor is available in the following packages:

• A 37.5 mm x 37.5 mm LGA package (LGA1151) for S-Processor Line

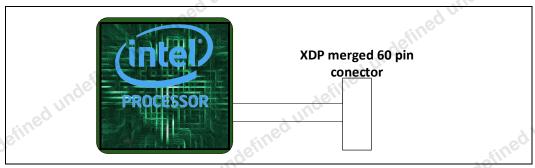
1.5 Processor Testability

An XDP on-board connector is a must to enable the processor full debug capabilities. For the processor SKUs, a merged XDP connector is highly recommended to enable lower C-state debug.

Note:

When separate XDP connectors will be used at C8 state, the processor will need to be waked up using the PCH.

Figure 1-2. Merged XDP Connector for Processor and PCH



The processor includes boundary-scan for board and system level testability.

1.6 Terminology

Table 1-2. Terminology (Sheet 1 of 3)

	Term	Description
	UHD	Ultra High Definition
, 0	AES	Advanced Encryption Standard
ineo	AGC	Adaptive Gain Control
d undefined b	BLT	Block Level Transfer
d Unit	ВРР	Bits per pixel
undefined th	CDR	Clock and Data Recovery
delli	CTLE	Continuous Time Linear Equalizer
4 uris	DDI	Digital Display Interface for DP or HDMI/DVI
80	DDR3	Third-generation Double Data Rate SDRAM memory technology



intel	76,		69,
	4 Unos	"gen"	efine
	e Veo	ad uli	
(Intel		Introduction	
Alle		unde defil!	
File		and the same of th	
Table 1-2.	Terminology (She	eet 2 of 3)	
ed un	Term	Description	
	DDR3L/RS	DDR3 Low Voltage Reduced Standby Power	
	DDR4/DDR4-RS	Fourth-Generation Double Data Rate SDRAM Memory Technology RS - Reduced Standby Power	ofined
	DFE	decision feedback equalizer	
	DMA	Direct Memory Access	
4 Uno	DMI	Direct Media Interface	
	DP	DisplayPort*	
deil.	DTS	Digital Thermal Sensor	
4 Une	ECC	Error Correction Code - used to fix DDR transactions errors	
ned undefined une	eDP*	embedded DisplayPort*	
	EU	Execution Unit in the Processor Graphics	
	GSA	Graphics in System Agent	
	HDCP	High-bandwidth Digital Content Protection	uger.
	HDMI*	High Definition Multimedia Interface	71.
nu.	IMC	Integrated Memory Controller	
· red	Intel [®] 64 Technology	64-bit memory extensions to the IA-32 architecture	
d undefile	Intel [®] DPST	Intel Display Power Saving Technology	
Unc	Intel [®] PTT	Intel Platform Trust Technology	
	Intel® TSX-NI	Intel Transactional Synchronization Extensions	
	Intel [®] TXT	Intel Trusted Execution Technology	
	Intel [®] VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.	define
Indefined ur	Intel [®] VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.	Ulli
	IOV	I/O Virtualization	
uge.	ISP	Image Signal Processor	
	LFM	Low Frequency Mode. corresponding to the Enhanced Intel SpeedStep® Technology's lowest voltage/frequency pair. It can be read at MSR CEh [47:40].	
	LLC	Last Level Cache	
	LPM	Low-Power Mode.The LPM Frequency is less than or equal to the LFM Frequency. The LPM TDP is lower than the LFM TDP as the LPM configuration limits the processor to single thread operation	adefil
	LPSP	Low-Power Single Pipe	4 all
ad u	LSF	Lowest Supported Frequency. This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions.	
adefine	MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].	
y un.	MLC	Mid-Level Cache	
	NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non- critical reserved balls/lands, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.	
	PAG	Platform Power Architecture Guide (formerly PDDG)	
ndefined undefined v	76.	Lowest Supported Frequency. This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions. Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48]. Mid-Level Cache Non-Critical to Function. NCTF locations are typically redundant ground or non-critical recogned balls/lands, so the loss of the colder joint continuity at end of life.	ad und



ndefined unde Table 1-2.

gem	16fine	ined	od um
	d undefin.	29611.	efine
		ad un.	ge
Introduction		(intel	
dum		inde.	
finec		ed d.	
Table 1-2.	Terminology (She	eet 3 of 3)	
ed U.	Term	Description	
ndefine	PCH IIIIde IIII	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as "chipset".	ofined uno
	PECI	Platform Environment Control Interface	Nge
	PEG	PCI Express Graphics	
4 Une	PL1, PL2, PL3	Power Limit 1, Power Limit 2, Power Limit 3	
	Processor	The 64-bit multi-core component (package)	1
indefined undefined un	Processor Core	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.	
lefine	Processor Graphics	Intel Processor Graphics	
Mos	PSR	Panel Self-Refresh	ed u
₽	Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SODIMM.	ndefine
•	SCI	System Control Interrupt. SCI is used in the ACPI protocol.	77.
Jefined undefined uno	SDP	Scenario Design Power. The Power consumed by a typical scenario. For more information, refer to the <i>Scenario Design Power (SDP) Implementation Considerations</i> document (see Related Documents section).	
4841110	SGX	Software Guard Extension	
Uno	SHA	Secure Hash Algorithm]
inea	SSC	Spread Spectrum Clock	
undefined undefined un	Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.	undefined un
, un	STR	Suspend to RAM	
ined	TAC	Thermal Averaging Constant	
defill	TCC	Thermal Control Circuit	
d Unit	TDP	Thermal Design Power	
inec.	ТОВ	Tolerance Budget	
nder.	TTV TDP	Thermal Test Vehicle TDP	undefined u
y m.	V _{CC}	Processor core power supply	FILES
	5551	Processor Graphics Power Supply	"uge,
	V _{CCIO}		30.
ed undefined undefined un	V _{CCSA}	System Agent Power Supply Vcc Sustain Power Supply	-
aned a	V _{CCST}		-
dein	V _{DDQ}	DDR Power Supply Variable Length Decoding	-
4 Une	VPID	Virtual Processor ID	-
sineu			-
"de"	. 22	200	J
9 111.	INOR	defil	Filler
	red v	4 Unit	"uge,
	ndefined undefin		od u.
	Inc	aden.	
Datasheet, Volun	ne 1 of 2	dull.	7
defil.		sines and us	
, und		nde.	
Jefined undefine		Processor Ground Processor Ground Indefined undefined	
16/11	44	ne d'e	



Table 1-3.

hed undefilie		· IInde
(intel)	Introduc	ction
I Those	adein	
afine ineo	ed un.	
1.7 Related Documents	Stines	
dulle	inge	
Table 1-3. Related Documents		
Document	Document Number/Location	
6th Generation Intel® Core Processor Family Datasheet, Volume 2 of 2	332688	
6th Generation Intel® Core Processor Family Specification Update	332689	
6th Generation Intel® Processor Platform I/O Datasheet, Volume 1 of 2	332690	
6th Generation Intel® Processor Platform I/O Datasheet, Volume 2 of 2	332691	
6th Generation Intel® Processor Platform I/O Specification Update	332692	
Advanced Configuration and Power Interface 3.0	http://www.acpi.info/	
DDR3 SDRAM Specification	http://www.jedec.org	
DDR4 Specification	http://www.jedec.org	-
High Definition Multimedia Interface specification revision 1.4	http://www.hdmi.org/manufacturer/specifi	-
Fash added Display Doubt Consideration revision 1.4	cation.aspx	
Embedded DisplayPort* Specification revision 1.4	http://www.vesa.org/vesa.standards/	_ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DisplayPort* Specification revision 1.2	http://www.vesa.org/vesa.standards/	400
PCI Express* Base Specification Revision 3.0	http://www.pcisig.com/specifications	-
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/ manuals/index.htm	
Totill,	20	
Totili,	20	
Intel® 64 and IA-32 Architectures Software Developer's Manuals § §	20	

18 Indefined undefined und



2 Interfaces

2.1 System Memory Interface

- Two channels of DDR3L/-RS and DDR4 memory with a maximum of two DIMMs per channel. DDR technologies, number of DIMMs per channel, number of ranks per channel are SKU dependent.
- UDIMM, SODIMM, and Memory Down support (based on SKU)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L/-RS I/O Voltage of 1.35V based on Processor Line
- DDR4 I/O Voltage of 1.2V
- 64-bit wide channels
- Non-ECC UDIMM and SODIMM DDR4/DDR3L/-RS support (based on SKU)
- Theoretical maximum memory bandwidth of:
 - 20.8 GB/s in dual-channel mode assuming 1333 MT/s
 - 25.0 GB/s in dual-channel mode assuming 1600 MT/s
 - 29.1 GB/s in dual-channel mode assuming 1866 MT/s
 - 33.3 GB/s in dual-channel mode assuming 2133 MT/s

Note: Memory down of all technologies (DDR3L/DDR4) should be implemented

homogeneously, which means that all DRAM devices should be from the same vendor and have the same part number. Implementing a mix of DRAM devices may cause

serious signal integrity and functional issues.

Note: If the S-Processor Line memory interface is configured to one DIMM per Channel, the processor can use either of the DIMMs, DIMM0 or DIMM1, signals CTRL[1:0] or

CTRL[3:2].

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3L/-RS and DDR4 protocols with two independent, 64-bit wide channels.

Table 2-1. Processor DRAM Support Matrix

S-Processor Line 2 1333/1600 1866/2133 N/A	Processor Line	DPC ¹	DDR3L/-RS	DDR4	LPDDR3
	S-Processor Line	2	1333/1600	1866/2133	N/A

Notes:

- DPC = DIMM Per Channel.
- Increasing the DDR4 rate to 2133 MT/s may lead to TDP power penalty up to 400mW, and 5-10% battery life impact.
- DDR3L/-RS Data Transfer Rates:
 - 1333 MT/s (PC3-10600)
 - 1600 MT/s (PC3-12800)
- DDR4 Data Transfer Rates:
 - 1866 MT/s (PC4-1866)
 - 2133 MT/s (PC4-2133)



• SODIMM Modules:

DDR3L/-RS SODIMM/UDIMM Modules:

 Standard 4-Gb technology and addressing are supported for x8 and x16 devices.

DDR4 SODIMM/UDIMM Modules:

 Standard 4-Gb and 8-Gb technologies and addressing are supported for x8 and x16 devices.

There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

- DDR3L/-RS Memory Down: Single and dual rank x8, x16 (based on SKU)
- DDR4 Memory Down: Single rank x8, x16 (based on SKU)

2.1.1.1 DDR3L/-RS Supported Memory Modules and Devices

Table 2-2. Supported DDR3L/-RS Non-ECC UDIMM Module Configurations (S-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Density	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
Α	4GB	4Gb	512M x 8	8	1	16/10	8	8K
В	8GB	4Gb	512M x 8	16	2	16/10	8	8K

Table 2-3. Supported DDR3L/-RS Non-ECC SODIMM Module Configurations (S-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Density	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
Α	4GB	4Gb	256M x 16	8	2	15/10	8	8K
В	4GB	4Gb	512M x 8	8	1	16/10	8	8K
С	2GB	4Gb	256M x 16	4	1	15/10	8	8K
F	8GB	4Gb	512M x 8	16	2	16/10	8	8K



2.1.1.2 DDR4 Supported Memory Modules and Devices

Table 2-4. Supported DDR4 Non-ECC UDIMM Module Configurations (S-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Density	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
Α	4GB	4Gb	512M x 8	8	1	15/10	16	8K
Α	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
В	8GB	4Gb	512M x 8	16	2	15/10	16	8K
В	16GB	8Gb	1024M x 8	16	2	16/10	16	8K
С	2GB	4GB	256M x 16	4	1	15/10	8	8K
С	4GB	8GB	512M x 16	4	1	16/10	8	8K

Table 2-5. Supported DDR4 Non-ECC SODIMM Module Configurations (S-Processor Line)

	Raw Card Version	DIMM Capacity	DRAM Device Density	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
	Α	4GB	4Gb	512M x 8	8	1	15/10	16	8K
	Α	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
	В	8GB	4Gb	512M x 8	16	2	15/10	16	8K
	В	16GB	8Gb	1024M x 8	16	2	16/10	16	8K
	С	2GB	4Gb	512M x 16	4	1	15/10	8	8K
	С	4GB	8Gb	512M x 16	4	1	16/10	8	8K
	E	8GB	4Gb	512M x 8	16	2	15/10	16	8K
Ī	E 0	16GB	8Gb	1024M x 8	16	2	16/10	16	8K

2.1.2 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- · Command Signal modes:
 - 1N indicates a new DDR3L/DDR4 command may be issued every clock
 - 2N indicates a new DDR3L/DDR4 command may be issued every 2 clocks



Table 2-6. DRAM System Memory Timing Support

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SODIMM Only)	CMD Mode
DDR3L/-RS	1333	8/9	8/9	8/9	7	1 or 2	1N/2N
DDROLJ RO	1600	10/11	10/11	10/11	8	1 or 2	1N/2N
DDR4	1866	12/13/14	12/13/14	12/13/14	10/12/12	1 or 2	1N/2N
DUNT	2133	14/15/16	14/15/16	14/15/16	11/14/14	1 or 2	1N/2N

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DDR Schema and DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

In this mode, all memory cycles are directed to a single channel. Single-Channel mode is used when either the Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel® Flex Memory Technology Mode

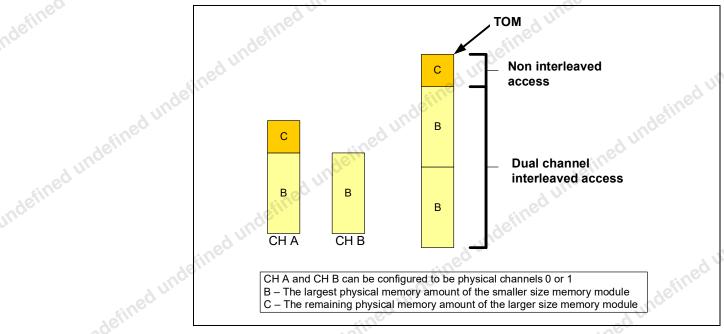
The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note:

Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa. However, channel A size must be greater or equal to channel B size.



Figure 2-1. Intel[®] Flex Memory Technology Operations



Dual-Channel Symmetric Mode (Interleaved Mode)

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For Dual-Channel modes both channels must have a DIMM connector populated. For Single-Channel mode, only a single channel can have a DIMM connector populated.



2.1.5 Technology Enhancements of Intel[®] Fast Memory Access

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.



undefined undefi

DDR I/O Interleaving

The processor supports I/O interleaving, which has the ability to swap DDR bytes for routing considerations. BIOS configures the I/O interleaving mode before DDR training.

There are 2 supported modes:

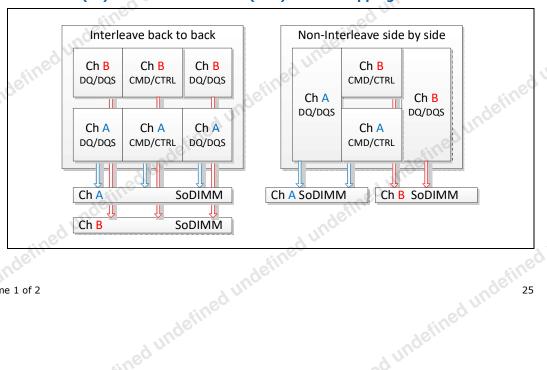
- Interleave (IL)
- Non-Interleave (NIL)

The following table and figure describe the pin mapping between the IL and NIL modes.

Table 2-7. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

Inde	I	L	2	N:	[L
Indefined unde	Channel	Byte	10	Channel	Byte
defille	DDR0	Byte0		DDR0	Byte0
11/10	DDR0	Byte1		DDR0	Byte1
	DDR0	Byte2		DDR0	Byte4
	DDR0	Byte3		DDR0	Byte5
undefined undefined unde	DDR0	Byte4		DDR1	Byte0
ed u	DDR0	Byte5		DDR1	Byte1
defille	DDR0	Byte6		DDR1	Byte4
unde	DDR0	Byte7		DDR1	Byte5
ineo	DDR1	Byte0		DDR0	Byte2
deff	DDR1	Byte1		DDR0	Byte3
Ulli	DDR1	Byte2		DDR0	Byte6
	DDR1	Byte3		DDR0	Byte7
2	DDR1	Byte4		DDR1	Byte2
, uno	DDR1	Byte5		DDR1	Byte3
ined	DDR1	Byte6		DDR1	Byte6
undefined und	DDR1	Byte7		DDR1	Byte7

Interleave (IL) and Non-Interleave (NIL) Modes Mapping





2.1.8 Data Swapping

By default, the processor supports on-board data swapping in two manners (for all segments and DRAM technologies):

- byte (DQ+DQS) swapping between bytes in the same channel.
- · bit swapping within specific byte.

2.1.9 DRAM Clock Generation

Every supported rank has a differential clock pair. There are a total of four clock pairs driven directly by the processor to DRAM.

2.1.10 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR3L/-RS and DDR4 Reference Voltage (VREF) internally for both read and write operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced training procedures in order to provide the best voltage to achieve the best signal margins.

2.2 PCI Express* Graphics Interface (PEG)

Note: The processor's PCI Express* interface is present only in 2-Chip platform processors.

This section describes the PCI Express* interface capabilities of the processor. See the PCI Express Base* Specification 3.0 for details on PCI Express*.

2.2.1 PCI Express* Support

The processor's PCI Express* interface is a 16-lane (x16) port that can also be configured as multiple ports at narrower widths (see Table 2-8, Table 2-9).

The processor supports the configurations shown in the following table.



PCI Express* Bifurcation and Lane Reversal Mapping

	Lit	nk Wid	th	Config. Signals			Lanes															
Bifurcation	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	17	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	(1)	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

- For CFG bus further details, refer to Section 6.4.
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.

For example:

- When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
- When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9. b.
- When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.
- For Reversal lanes, For example:
 - When using 1x8, the 8 lane device must use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
 - When using 1x4, the 4 lane device must use lanes 12:15, so lane 15 will be connected to lane 0 of the Device.
 - When using 1x2, the 4 lane device must use lanes 14:15, so lane 15 will be connected to lane 0 of the Device.

The processor supports the following:

- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset.
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0: DMI -> PCI Express* Port 0
- 64-bit downstream address format, but the processor never generates an address above 512 GB (Bits 63:39 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 512 GB (addresses where any of Bits 63:39 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 512 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- PCI Express* reference clock is 100-MHz differential clock
- Power Management Event (PME) functions
- Dynamic width capability



- Message Signaled Interrupt (MSI and MSI-X) messages
- · Lane reversal
- Full Advance Error Reporting (AER) and control capabilities

The following table summarizes the transfer rates and theoretical bandwidth of PCI Express* link.

Table 2-9. PCI Express* Maximum Transfer Rates and Theoretical Bandwidth

PCI Express*	Encoding	Maximum Transfer Rate	Theoretical Bandwidth [GB/s]									
Gen	Encouning	[GT/s]	x1	x2	x4	x8	x16					
Gen 1	8b/10b	2.5	0.25	0.5	1.0	2.0	4.0					
Gen 2	8b/10b	5	0.5	1.0	2.0	4.0	8.0					
Gen 3	128b/130b	8	1.0	2.0	3.9	7.9	15.8					

Note: The processor has limited support for Hot-Plug, for details refer to Section 4.4.

2.2.2 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express* configuration uses standard mechanisms as defined in the PCI Plug and-Play specification. The processor PCI Express* ports support Gen 3. At 8 GT/s, Gen 3 operation results in twice as much bandwidth per lane as compared to Gen 2 operation. The 16 lanes port can operate at 2.5 GT/s, 5 GT/s, or 8 GT/s.

Gen 3 PCI Express* uses a 128b/130b encoding which is about 23% more efficient than the 8b/10b encoding used in Gen 1 and Gen 2.

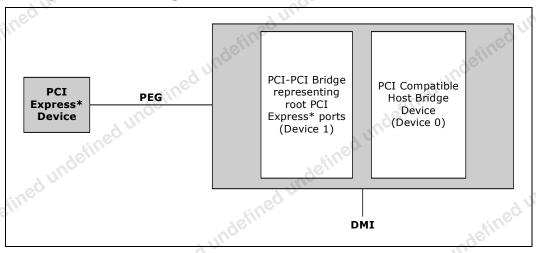
The PCI Express* architecture is specified in three layers – Transaction Layer, Data Link Layer, and Physical Layer. See the *PCI Express Base Specification 3.0* for details of PCI Express* architecture.



2.2.3 PCI Express* Configuration Mechanism

The PCI Express* (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 2-3. PCI Express* Related Register Structures in the Processor



PCI Express* extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the conventional PCI specification. PCI Express* configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express* region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express* configuration access mechanism described in the PCI Express* Enhanced Configuration Mechanism section.

The PCI Express* Host Bridge is required to translate the memory-mapped PCI Express* configuration space accesses from the host processor to PCI Express* configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the PCI Express Base Specification for details of both the PCI-compatible and PCI Express* Enhanced configuration mechanisms and transaction rules.

2.2.4 PCI Express* Equalization Methodology

The equalization of link requires equalization for both TX and RX sides for the processor and for the End point device.

Adjusting transmitter and receiver of the lanes is done to improve signal reception quality and for improving link robustness and electrical margin.

The link timing margins and voltage margins are strongly dependent on equalization of the link.

The processor supports the following:

 Full TX Equalization: Three Taps Linear Equalization (Pre, Current and Post cursors), with FS/LF (Full Swing /Low Frequency) 24/8 values respectively.



- Full RX Equalization and acquisition for: AGC (Adaptive Gain Control), CDR (Clock and Data Recovery), adaptive DFE (decision feedback equalizer) and adaptive CTLE peaking (continuous time linear equalizer).
- Full adaptive phase 3 EQ compliant with PCI Express* Gen 3 specification

See the PCI Express* Base Specification 3.0 for details on PCI Express* equalization.

2.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH.

Main characteristics:

- 4 lanes Gen 3 DMI support
- 8 GT/s point-to-point DMI interface to PCH
- DC coupling no capacitors between the processor and the PCH
- · PCH end-to-end lane reversal across the link
- Half-Swing support (low-power/low-voltage)

Note: Only DMI x4 configuration is supported.

Note: Polarity Inversion on DMI Link is not allowed on both sides of the processor and the

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors; never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.2 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics

The processor graphics is based on GEN 9 (generation 9) graphics core architecture that enables substantial gains in performance and lower-power consumption over prior generations. GEN 9 architecture supports up to 72 Execution Units (EUs), depending on the processor SKU.

The new processor graphics architecture delivers high dynamic range of scaling to address segments spanning low power to high power, increased performance per watt, support for next generation of APIs and extends heterogeneous programmability with IA core/GPU and Shared Virtual memory (SVM). GEN 9 scalable architecture is partitioned by usage domains along Render/Geometry, Media, and Display. The



architecture also delivers very low-power video playback and next generation analytics and filters for imaging related applications. The new Graphics Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and "PCI-like" traffic in and out.

The display engine supports the latest display standards such as eDP* 1.3, DP* 1.2, HDMI* 1.4, HW support for blend, scale, rotate, compress, high PPI support, and advanced SRD2 display power management.

2.4.1 API Support (Windows*)

- Direct3D* 12, Direct3D* 11.3, Direct3D* 11.2, Direct3D 11.1, Direct3D 9, Direct3D 10, Direct2D
- OpenGL* 4.4
- OpenCL* 2.1, OpenCL* 2.0, OpenCL* 1.2

Direct3D* 11.x extensions:

• PixelSync, InstantAccess.

Gen 9 architecture delivers hardware acceleration of Direct X* 11 Render pipeline comprising of the following stages: Vertex Fetch, Vertex Shader, Hull Shader, Tesselation, Domain Shader, Geometry Shader, Rasterizer, Pixel Shader, Pixel Output. The Direct X* 12 API is supported at feature level 12_1.

2.4.2 Media Support (Intel[®] QuickSync & Clear Video Technology HD)

GEN 9 implements multiple media video codecs in hardware as well as a rich set of image processing algorithms.

Note: All supported media codecs operate on 8 bpc, YCbCr 4:2:0 video profiles.

2.4.2.1 Hardware Accelerated Video Decode

GEN 9 implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW decode is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2)
- Direct3D11 Video API
- Intel Media SDK
- MFT (Media Foundation Transform) filters.

GEN 9 supports full HW accelerated video decoding for AVC/VC1/MPEG2/HEVC/VP8/JPEG.

Note: HEVC – 8 bit support.



Table 2-10. Hardware Accelerated Video Decoding

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	Main High	1080p
VC1/WMV9	Advanced Main Simple	L3 High Simple	3840×3840
AVC/H264	High Main MVC & stereo	L5.1	2160p(4K)
VP8	0	Unified level	1080p
JPEG/MJPEG	Baseline	Unified level	16k x16k
HEVC/H265	Main	L5.1	2160(4K)
VP9*	0 (4:2:0 Chroma 8-bit)	Unified level	ULT, 4k 24fps @15Mbps ULX, 1080p 30fps @ 10Mbps
	MPEG2 VC1/WMV9 AVC/H264 VP8 JPEG/MJPEG HEVC/H265	MPEG2 Main Advanced Main Simple AVC/H264 AVC/H264 Main MVC & stereo VP8 0 JPEG/MJPEG Baseline HEVC/H265 Main	MPEG2 Main Main High Advanced Main Simple AVC/H264 AVC/H264 Main Moin Moin Moin Moin Moin Moin Moin Mo

Expected performance:

More than 16 simultaneous decode streams @ 1080p.

Note:

Actual performance depends on the processor SKU, content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

2.4.2.2 **Hardware Accelerated Video Encode**

GEN 9 implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW encode is exposed by the graphics driver using the following APIs:

- Intel Media SDK
- MFT (Media Foundation Transform) filters

GEN 9 supports full HW accelerated video encoding for AVC/MPEG2/HEVC/VP8/JPEG.

Table 2-11. Hardware Accelerated Video Encode

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	High	1080p
AVC/H264	Main High	L5.1	2160p(4K)
VP8	Unified profile	Unified level	_
JPEG	Baseline	/e,, –	16Kx16K
HEVC/H265	Main	L5.1	2160p(4K)
VP9	Support 8 bits 4:2:0 BT2020 may be obtained the pre/ post processing	_	4efined b

Hardware decode for H264 SVC is not supported.

indefined undefined undefined in Datasheet, Volume 1 of 2



2.4.2.3 Hardware Accelerated Video Processing

There is hardware support for image processing functions such as De-interlacing, Film cadence detection, Advanced Video Scaler (AVS), detail enhancement, image stabilization, gamut compression, HD adaptive contrast enhancement, skin tone enhancement, total color control, Chroma de-noise, SFC pipe (Scalar and Format Conversion), memory compression, Localized Adaptive Contrast Enhancement (LACE), spatial de-noise, Out-Of-Loop De-blocking (from AVC decoder), 16 bpc support for de-noise/de-mosaic.

There is support for Hardware assisted Motion Estimation engine for AVC/MPEG2 encode, True Motion, and Image stabilization applications.

The HW video processing is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2).
- Direct3D 11 Video API.
- Intel Media SDK.
- MFT (Media Foundation Transform) filters.
- Intel CUI SDK.

Note: Not all features are supported by all the above APIs. Refer to the relevant documentation for more details.

2.4.2.4 Hardware Accelerated Transcoding

Transcoding is a combination of decode video processing (optional) and encode. Using the above hardware capabilities can accomplish a high-performance transcode pipeline. There is not a dedicated API for transcoding.

The processor graphics supports the following transcoding features:

- Low-power and low-latency AVC encoder for video conferencing and Wireless Display applications.
- Lossless memory compression for media engine to reduce media power.
- HW assisted Advanced Video Scaler.
- Low power Scaler and Format Converter.

Expected performance:

• S-Processor Line: 18x 1080p30 RT (same as previous generation).

Note: Actual performance depends on Processor Line, video processing algorithms used, content bit rate, and memory frequency.

2.4.3 Camera Pipe Support

Camera pipe functions such as de-mosaic, white balance, defect pixel correction, black level correction, gamma correction, LGCA, vignette control, Front end Color Space Converter (CSC), Image Enhancement Color Processing (IECP).



2.4.4 Switchable/Hybrid Graphics

The processor supports Switchable/Hybrid graphics.

Switchable graphics: The Switchable Graphics feature allows you to switch between using the Intel integrated graphics and a discrete graphics card. The Intel Integrated Graphics driver will control the switching between the modes. In most cases it will operate as follows: when connected to AC power - Discrete graphic card; when connected to DC (battery) - Intel integrated Graphics

Hybrid graphics: Intel integrated graphics and a discrete graphics card work cooperatively to achieve enhanced power and performance.

Table 2-12. Switchable/Hybrid Graphics Support

Operating System	Hybrid Graphics	Switchable Graphics ²
Windows* 7	N/A	Yes ¹
Windows* 8.1	Yes ¹	N/A
Windows* 10	Yes ¹	N/A

Note:

- 1. Contact your graphics vendor to check for support.
- 2. Intel does not validate any SG configurations on Win8.1 or Win10.

2.4.5 GEN 9 Video Analytics

There is HW assist for video analytics filters such as scaling, convolve 2D/1D, minmax, 1P filter, erode, dilate, centroid, motion estimation, flood fill, cross correlation, Local Binary Pattern (LBP).

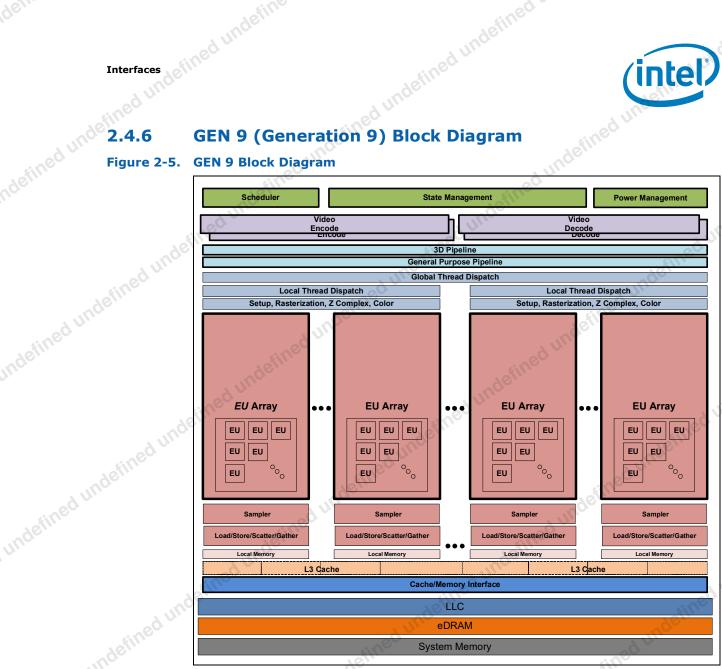
Figure 2-4. Video Analytics Common Use Cases

						440					
undefined undefined ur	Usage	Scaling	Convolve 2D / 1D	MinMax Filter	Erode Dilat	e Centroid	Motion Estimation	Floodfill	Cross Correlation	LBP Creation	
od ni,	Face Detection									961	
Fine	Face Expressions			e					1		
age,	Face Recognition		117						"Veo		
4 Ull.	Face Tracking		OT.								
•	Gesture Detection	79									
	Gesture Tracking	16					69				
	Scene Identification			Ī			Silving				
	2D to 3D Video			Ī							
	Object Detection					9.1					
	Object Tracking					e					
. 0	Video Enhancement				78/6/1						
ed.	Video Segmentation				71,					1000	
1efill	Visual Search			2					6-	O.	
inoc	Stereo		I e						2/12		
0.	Superes		71					60.	S		
		-00A					-	711,			
o'	16										
Jefined undefined v	Inoc						Ye				
						, un					



GEN 9 (Generation 9) Block Diagram

GEN 9 Block Diagram



d undefined undefined und **GT2 Graphics Frequency**

GT2 Graphics Frequency (S-Processor Line) Table 2-13.

adefined		ined un.		sined unoc			
Inde		T2 Graphics Fred T2 Graphics Frequency		, nuger,		4 undefined !	
	Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice	GT Unslice + 3 GT Slice	30	
	S - quad core	GT2 GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	_	ed_um		
"sed"	S - dual core	GT2 GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	_	defin -		
ed undefilm	Datasheet, Volume 1	efined undefines	undefin	undefined undefined the			
lefined	Datasneet, volume 1	ined u	ndefined L	ران م	Indefined unc	35	



2.5 Display Interfaces

The processor supports single eDP* interface and 2 or 3 DDI interfaces (depends on segment):

- DDI interface can be configured as DisplayPort* or HDMI*.
- Each DDI can support dual mode (DP++).
- Each DDI can support DVI (DVI maximum resolution is 1920x1200 @ 60 Hz).
- The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate.
- DDI ports notated as: DDI B, C, D.
- S-Processor Line processors supports eDP and up to 3 DDI supporting DP/HDMI.
- AUX/DDC signals are valid for each DDI Port. (Three for S-Processor Line)
- Total Five dedicated HPD (Hot-plug detect signals) are valid for all processor SKUs.

Note: SSC is supported in eDP*/DP for all Processor Lines.

- Digital Display InterfaceDDI ports (B, C, and D) are disabled if No Connect Pull-Up resistor on following PCH signals: DDPB_CTRLDATA, DDPC_CTRLDATA and DDPD_CTRLDATA accordingly.
- eDP* port is Disabled if No Connect Pull-Down resistor on CFG[4]
- SW strap can override HW strap.

Note: The processor platform supports DP Type-C implementation with additional discrete

components.

Note:

- eDP* bifurcation:
 - eDP bifurcation for S-Processor Line can be used for: DP x2 upper lanes (DDIE) for VGA support and eDP x2 lower lanes. Both eDP ports can be used simultaneously.

Table 2-14. VGA and embedded DisplayPort* (eDP*) Bifurcation Summary

Port Unit	S-Processor Line (DT)			
eDP - DDIA (eDP lower x2 lanes, [1:0])	No No			
VGA - DDIE (DP upper x2 lanes, [3:2])	Yes ¹			

Notes:

- 3. Requires a DP to VGA converter
- DP-to-VGA converter on processor DDI ports is supported using External Dongle only, display driver software treat these VGA dongles as a DP Branch device

The technologies supported by the processor are listed in the following table.



Table 2-15. embedded DisplayPort* (eDP*)/DDI Ports Availability

adefine	Ports	Port name in VBT	S-Processor Line (DT) ^{2,3}
	DDIO - eDP	Port A	Yes
	DDI1	Port B	Yes
34	DDI2	Port C	Yes
uno	DDI3	Port D	Yes
ined .	DDI4 - eDP	Port E	Yes ¹
Indefined undefin	 a. For example, DT car must be used as DD 2. 3xDDC (DDPB, DDPC, DDPD 3. 5xHPD (PCH) inputs (eDP_Hi processor SkUs. 4. DDI3_AUX are exists as rese 5. VBT provides a configuration 	nuse eDP_AUX for VGA conver PE_HPD3.) are valid for all processor SK PD, DDPB_HPD0, DDPC_HPD1. rved.	, DDPD_HPD2, DDPE_HPD3) are valid for all channels A/B/C/D for a given port, based on

Notes:

- Port E is bifurcated from eDP. When VGA is used, need to use available AUX (if HDMI is in used).
 - For example, DT can use eDP_AUX for VGA converter which is available as free Design but HPD must be used as DDPE_HPD3.
- 3xDDC (DDPB, DDPC, DDPD) are valid for all processor SKUs).
- 5xHPD (PCH) inputs (eDP_HPD, DDPB_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all processor SKUs.
- 4. DDI3_AUX are exists as reserved.
- VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board

Table 2-16. Display Technologies Support

Technology	Standard		
eDP* 1.3	VESA* Embedded DisplayPort* Standard 1.3		
DisplayPort* 1.2	VESA DisplayPort* Standard 1.2 VESA DisplayPort* PHY Compliance Test Specification 1.2 VESA DisplayPort* Link Layer Compliance Test Specification 1.2		
HDMI* 1.4 ¹	High-Definition Multimedia Interface Specification Version 1.4		

- HDMI* 2.0 support is possible using LS-Pcon converter chip connected to the DP* port. The LS-Pcon supports 2 modes:
 - Level shifter for HDMI 1.4 resolutions.
 - DP-HDMI 2.0 protocol converter for HDMI 2.0 resolutions.
- The HDMI* interface supports HDMI with 3D, 4Kx2K @24 Hz, Deep Color, and x.v.Color.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high definition content playback over digital interfaces, HDCP is not supported for eDP.
- The processor supports eDP* display authentication: Alternate Scrambler Seed Reset (ASSR).
- The processor supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector. The maximum MST DP supported resolution for S-Processor Line is shown in the following table.

. A . madefined undefined undefined Datasheet, Volume 1 of 2



Table 2-17. Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations

			7 //,			
ndefill	Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]	
undefined undefined undefin	640	480	60	25.2	0.76	
iefil.	800	600	60	40	1.20	
	1024	768	60	65	1.95	
od v.	1280	720	60	74.25	2.23	
	1280	768	60	68.25	2.05	
ader	1360	768	60	85.5	2.57	
d Ulli	1280	1024	60	108	3.24	
	1400	1050	60	101	3.03	
defil	1680	1050	60	119	3.57	
	1920	1080	60	148.5	4.46	
		1200	60	154	4.62	
	2048	1152	60	156.75	4.70	
16,11	2048	1280	60	174.25	5.23	
ino	2048	1536	60	209.25	6.28	
	2304	1440	60	218.75	6.56	
	2560	1440	60	241.5	7.25	
age.	3840	2160	30	262.75	7.88	
4 mi	2560	1600	60	268.5	8.06	
	2880	1800	60	337.5	10.13	
Jeill.	3200	2400	60	497.75	14.93	
undefined undefined undefi	3840	2160	60	533.25	16.00	
	4096	2160	60	556.75	17.02	
	4096	2304	60	605	18.15	
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			1		

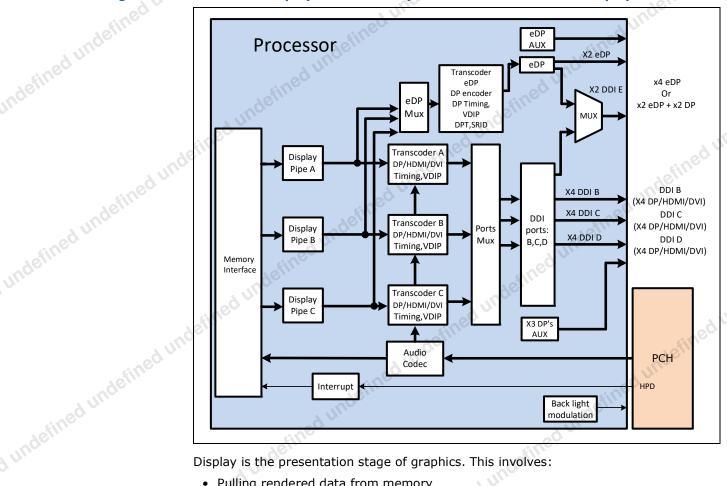
Notes:

- 1. All above is related to bit depth of 24.
- The data rate for a given video mode can be calculated as: Data Rate = Pixel Frequency * Bit Depth.
- The bandwidth requirements for a given video mode can be calculated as: Bandwidth = Data Rate * 1.25 (for 8B/10B coding overhead).
- 4. The Table above is partial List of the common Display resolutions just for example. The Link Bandwidth depends if the standards is Reduced Blanking or not. If the Standard is Not reduced blanking the expected Bandwidth will be higher. For more details refer to VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT). Version 1.0, Rev. 13 February 8, 2013 To calculate what are the resolutions that can be supported in MST configurations, follow the below guidelines:
 - Identify what is the Link Bandwidth (column right) according the requested Display resolution.
 - Summarize the Bandwidth for Two of three Displays accordingly, and make sure the final result is below 21.6Gbps. (for HBR2, four lanes)
 - For special cases when x2 lanes are used or HBR or RBR used , refer to the tables in Section 2.5.11 accordingly.
- 5. For examples:
 - a. Docking Two displays: 3840x2160@60hz + 1920x1200@60hz = 16 + 4.62 = 20.62Gbps [Supported]
 - b. Docking Three Displays: 3840x2160@30hz + 3840x2160@30hz + 1920x1080@60hz = 7.88 + 7.88 + 4.16 = 19.92Gbps [Supported]
- 6. Consider also the supported resolutions as mentioned in Section 2.5.6 and Section 2.5.7.
- The processor supports only 3 streaming independent and simultaneous display combinations of DisplayPort*/eDP*/HDMI*/DVI monitors. In the case where 4 monitors are plugged in, the software policy will determine which 3 will be used.



- Three High Definition Audio streams over the digital display interfaces are
- For display resolutions driving capability see Table 2-19.
- ndefined undefined undefined undefine DisplayPort* Aux CH supported by the processor, while DDC channel, Panel power sequencing, and HPD are supported through the PCH. Refer to the appropriate Platform Controller Hub (PCH) Datasheet (see related documents) for more information.

Figure 2-6. Processor Display Architecture (with 3 DDI Ports as an Example)



Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard



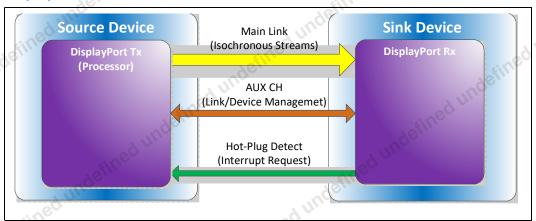
2.5.1 DisplayPort*

The DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance to VESA* DisplayPort* specification. Refer to Table 2-16.

Figure 2-7. DisplayPort* Overview



2.5.2 High-Definition Multimedia Interface (HDMI*)

The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

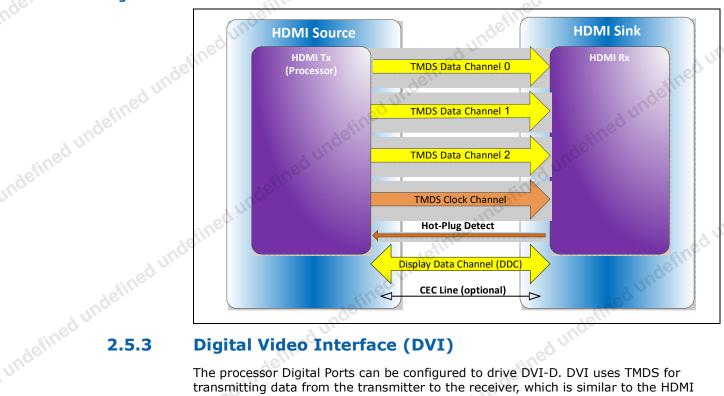
HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.



The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface.

Figure 2-8. **HDMI*** Overview



Digital Video Interface (DVI)

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol except for the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. The digital display data signals driven natively through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

embedded DisplayPort* (eDP*)

The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal. eDP* can be bifurcated in order to support VGA display.

Integrated Audio 2.5.5

- HDMI* and display port interfaces carry audio along with video.
- The processor supports 3 High Definition audio streams on 3 digital ports simultaneously (the DMA controllers are in PCH).
- The integrated audio processing (DSP) is performed by the PCH, and delivered to . 4 . indefined undefined undefined the processor using the AUDIO SDI and AUDIO CLK inputs pins.
- AUDIO_SDO output pin is used to carry responses back to the PCH
- Supports only the internal HDMI and DP CODECs.



Table 2-18. Processor Supported Audio Formats over HDMI* and DisplayPort*

	Audio Formats	HDMI*	DisplayPort*
	AC-3 Dolby* Digital	Yes	Yes
	Dolby Digital Plus	Yes	Yes
	DTS-HD*	Yes	Yes
	LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
ed un	Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes
defined undefine	The processor will continue to support Silent st audio feature that enables short audio streams over the HDMI* and DisplayPort* monitors. The the HDMI and DisplayPort interfaces at 44.1 kHz and 192 kHz sampling rates.	, such as system ever processor supports	vents to be heard s silent streams over

2.5.6 Multiple Display Configurations (Dual Channel DDR)

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort/HDMI/DVI. The following table shows examples of valid three display configurations through the processor.

Table 2-19. Display Resolution (Sheet 1 of 2)

- ned		110		
defill	Standard	S-Processor Line (Display 1,2,3,4)	Notes	, 0
Jundefined	eDP*	4096x2304 @ 60Hz, 24bpp	1, 2, 3	ined.
D	DP*	4096x2304 @ 60Hz, 24bpp	1, 2, 3	defill.
λ	HDMI* 1.4 (native)	4096x2160 @ 24 Hz, 24 bpp	1, 2, 3	Jundefined u
dun	HDMI 2.0 (Via LS-Pcon)	4096x2160 @ 60Hz, 24bpp	1, 2, 3, 7	
ad undefined undefined v	(Via LS-Pcon)	Stineo	raed un.	
sed une	d un	defined undefined undefine	efil.	
define	iefineo	ined un		-61
ed un.	4 unde	indefin		ed undefined
	iefines.	ined u.		duna
d un		inde ^{it}	4efine	
42		D D	atasheet, Volume 1 of 2	
inder		4efine	eined a	
raed ur	A UI	,,0	ger.	
Jefill"	sined	ad u''		



Table 2-19. Display Resolution (Sheet 2 of 2)

Standard	S-Processor Line (Display 1,2,3,4)	Notes
----------	------------------------------------	-------

Notes:

- 1. Maximum resolution is based on implementation of 4 lanes with HBR2 link data rate.
- 2. bpp bit per pixel.
- 3. S-processors support up to 4 displays but only three can be active at the same time.
- The resolutions are assumed at max VCC_{SA}, additional power penalty of ~0.26W per one Display Port. Final resolutions depends on overall power specifications/limitations.
- 5. In case of connecting more than one active display port the processor frequency may be lower than base frequency at thermally limited scenario.
- Supporting 4K display required two DDR channels of same size. Performance degradations exists in SKL
 platforms while running 4K content for system using single channel system memory (compared to using
 dual channel).
- HDMI2.0 implemented using LSPCON device. Only one LSPCON with HDCP2.2 support is supported per processor platform.

2.5.7 Multiple Display Configurations (Single Channel DDR)

Table 2-20. S-Processor Line Display Resolution Configuration

	dine	Maximum Resolution (Clone/ Extended Mode)		
ined uni	Minimum DDR Speed [MT/s]	eDP @60 Hz (Primary)	DP @ 60 Hz / HDMI ¹ @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI ¹ @ 30 Hz (Secondary 2)
defill	1222	4096 x 2304	Not Connected	Not Connected
4 Une	1333	2560 x 1440	4096 x 2304	Not Connected
	1600	3840 x 2160	4096 x 2304	Not Connected
gel.	1866	2560 x 1440	4096 x 2304	4096 x 2304
	2133	3840 x 2160	4096 x 2304	4096 x 2304

Table 2-21. S-Processor Line Display Resolution Configuration when DP @ 30 Hz

Minimum DDR	Maximum Resolution (Clone/ Extended mode)			
Speed [MT/s]			DP @30 Hz (Secondary 2)	
1333	3840x 2160	Not Connected	Not Connected	
1333	3840 x 2160	4096 x 2304	Not Connected	
1600	3840 x 2160	4096 x 2304	4096 x 2304	

2.5.8 High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 1.4 for content protection over wired or wireless displays (HDMI*, DVI, and DisplayPort*).

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.



Table 2-22. HDCP Display supported Implications

Displa	y Support	Content Protection Implications
HDCD 104	HDMI 1.4	Native FHD Only
HDCP 1.4	Display Port	Native FHD Only
4ines	HDMI 1.4	LSPCON UHD 2160p30
HDCP 2.2	HDMI 2.0	LSPCON UHD 2160p60
	HDMI 2.0a	Not Supported
	Display Port	Not Supported

2.5.9 Display Link Data Rate Support

Table 2-23. Display Link Data Rate Support

Technology	Link Data Rate
eDP*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
DisplayPort*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
HDMI*	2.97 Gb/s

Table 2-24. Display Resolution and Link Rate Support

Resolution	Link Rate Support	High Definition		
4096x2304	5.4 (HBR2)	UHD (4K)		
3840x2160	5.4 (HBR2)	UHD (4K)		
3200x2000	5.4 (HBR2)	QHD+		
3200x1800	5.4 (HBR2)	QHD+		
2880x1800	2.7 (HBR)	QHD		
2880x1620	2.7 (HBR)	QHD		
2560x1600	2.7 (HBR)	QHD		
2560x1440	2.7 (HBR)	QHD		
1920×1080	1.62 (RBR)	FHD		

2.5.10 Display Bit Per Pixel (BPP) Support

Table 2-25. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24, 30, 36
DisplayPort*	24, 30, 36
HDMI*	24, 36



Display Resolution per Link Width 2.5.11

Table 2-26. Supported Resolutions for HBR2 (5.4Gbps) by Link Width

Link Width	Max. Link Bandwidth [Gbps]	Max. Pixel Clock (Theoretical) [MHz]	S-Processor Line	
4 lanes	21.6	720 ²	See Table 2-19	
2 lanes	10.8	360	2880x1800@60Hz, 24bpp	
1 lane	5.4	180	2048x1280@60Hz, 24bpp	

Notes:

- The examples assumed 60 Hz refresh rate and 24 bpp.
- The actual Max pixel clock for HBR2 is limited by the CD clock to 675 MHz for S-Processor Line.

Table 2-27. Supported Resolutions for HBR (2.7Gbps) by Link Width

Link Width	Max. Link Bandwidth [Gbps]	Max. Pixel Clock (Theoretical) [MHz]	S-Processor Line	
4 lanes	10.8	360	2880x1800@60Hz, 24bpp	
2 lanes	5.4	180	2048x1280@60Hz, 24bpp	
1 lane	2.7	90	1280x960@60Hz, 24bpp	
Notes	20	•		

undefined undefined unde **Platform Environmental Control Interface (PECI)**

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

The examples assumed 60 Hz refresh rate and 24 bpp.



2.6.1 **PECI Bus Architecture**

The PECI architecture is based on a wired OR bus that the clients (as processor PECI) can pull up (with strong drive).

The idle state on the bus is near zero.

The following figures demonstrates PECI design and connectivity:

- PECI Host-Clients Connection: While the host/originator can be third party PECI host and one of the PECI client is a processor PECI device.
- PECI EC Connection.

Example for PECI Host-Clients Connection Figure 2-9.

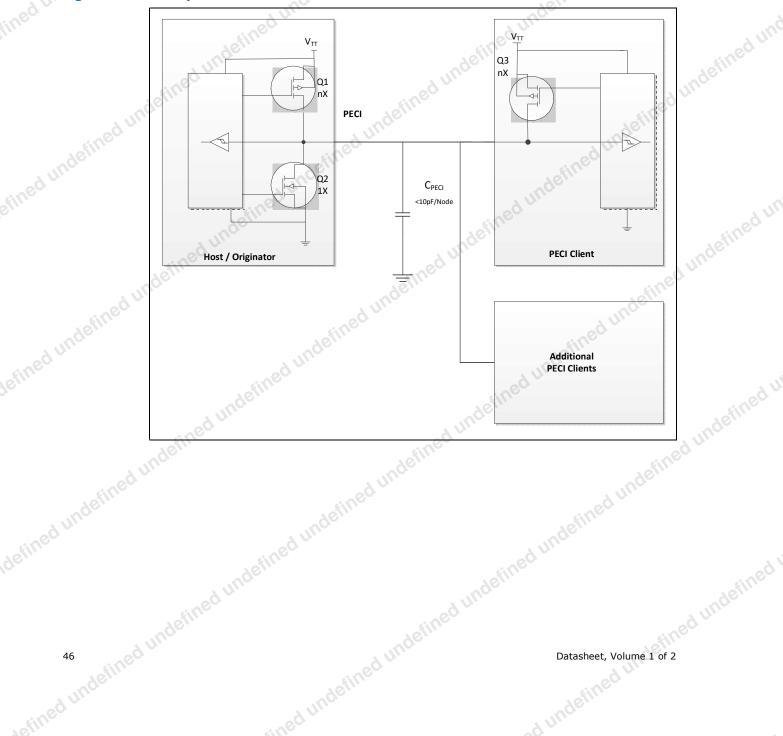
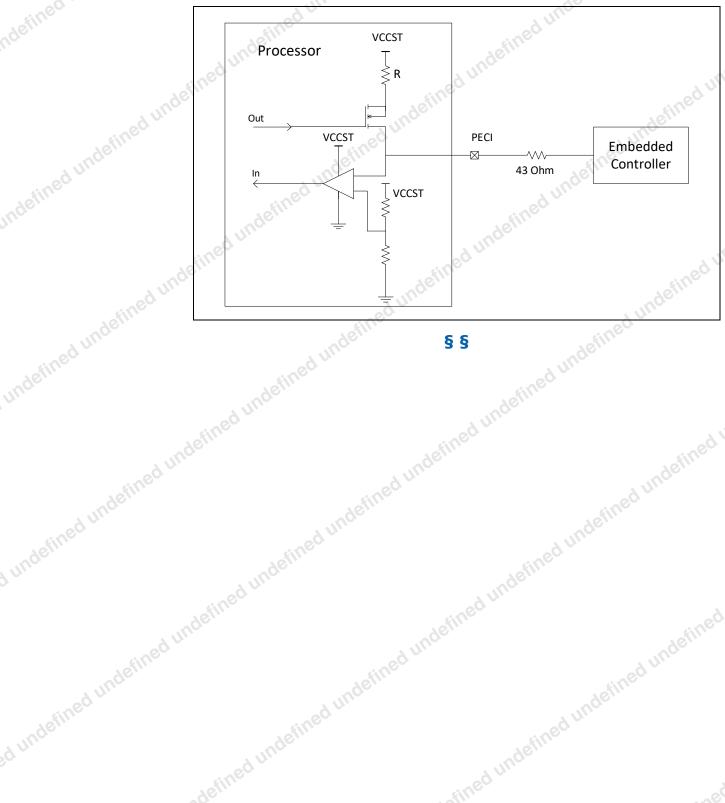




Figure 2-10. Example for PECI EC Connection



nume 1 of 2 Datasheet, Volume 1 of 2 istined undefi



3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel[®] Virtualization Technology (Intel[®] VT)

Intel[®] Virtualization Technology (Intel[®] VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel[®] Virtualization Technology (Intel[®] VT) for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel[®] Virtualization Technology for Directed I/O (Intel[®] VT-d) extends Intel VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel® VT-x specifications and functional descriptions are included in the *Intel*® *64 and IA-32 Architectures Software Developer's Manual, Volume 3*. Available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel[®] Virtualization Technology (Intel[®] VT) for IA-32, Intel[®] 64 and Intel[®] Architecture (Intel[®] VT-X)

Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- Robust: VMMs no longer need to use para-virtualization or binary translation. This
 means that VMMs will be able to run off-the-shelf operating systems and
 applications without any special steps.
- Enhanced: Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation
 of VMs and further prevents corruption of one VM from affecting others on the
 same system.



Intel® VT-x Key Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
 - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as defragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- EPTP (EPT pointer) switching
 - EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
 - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor IA core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
 - EPT is hardware assisted page table virtualization
 - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
 - Ability to assign a VM ID to tag processor IA core hardware structures (such as TLBs)
 - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- · Guest Preemption Timer
 - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
 - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
 - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
 - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.



3.1.2 Intel[®] Virtualization Technology (Intel[®] VT) for Directed I/O (Intel[®] VT-d)

Intel® VT-d Objectives

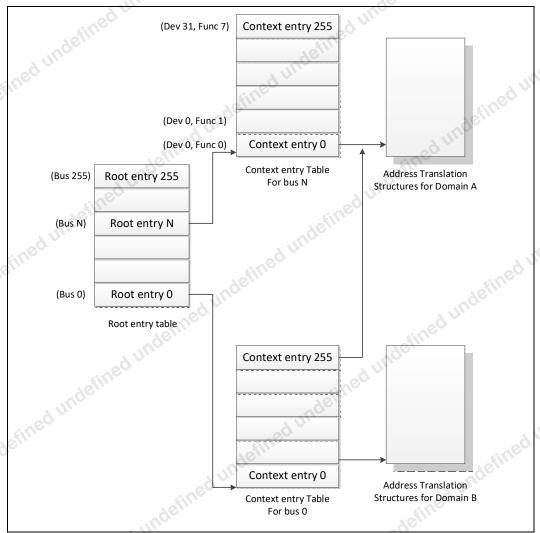
The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.
- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.



Figure 3-1. Device to Domain Mapping Structures



Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express* host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to *Intel Virtualization Technology for Directed I/O Architecture Specification* http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/vt-directed-io-spec.pdf



Intel® VT-d Key Features

The processor supports the following Intel VT-d features:

- Memory controller and processor graphics comply with the Intel VT-d 2.1 Specification.
- Two Intel VT-d DMA remap engines.
 - iGFX DMA remap engine
 - Default DMA remap engine (covers all devices except iGFX)
- · Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- · Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx xxxxh) not translated
 - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- · Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk both default Intel VT-d engine as well as the IGD VT-d engine are upgraded to support 4-level Intel VT-d tables (adjusted guest address width of 48 bits)
- Intel VT-d superpage support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD)
 IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel VT-d engine when iGfx is enabled.

Note: Intel VT-d Technology may not be available on all SKUs.



3.2 Security Technologies

3.2.1 Intel[®] Trusted Execution Technology (Intel[®] TXT)

Intel Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs, both VLWs and IPI

For the above features, BIOS must test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the Intel® Trusted Execution Technology Measured Launched Environment Programming Guide

Note: Intel TXT Technology may not be available on all SKUs.



3.2.2 Intel[®] Advanced Encryption Standard New Instructions (Intel[®] AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

Note: Intel AES-NI Technology may not be available on all SKUs.

3.2.3 PCLMULQDQ (Perform Carry-Less Multiplication Quadword) Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.2.4 Intel[®] Secure Key

The processor supports Intel Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

3.2.5 Execute Disable Bit

The Execute Disable Bit allows memory to be marked as non executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system.

See the *Intel 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.



3.2.6 Boot Guard Technology

Boot Guard technology is a part of boot integrity protection technology. Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Boot Guard accomplishes this by:

- Providing of hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing of architectural definition for platform manufacturer Boot Policy.
- Enforcing of manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer's hardware to run an unauthorized software stack.

Note: Boot Guard availability may vary between the different SKUs.

3.2.7 Supervisor Mode Execution Protection (SMEP)

Intel[®] Supervisor Mode Execution Protection (SMEP) is a mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to *Intel*[®] 64 and *IA-32 Architectures Software Developer's Manual*, *Volume 3A* at: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.8 Intel Supervisor Mode Access Protection (SMAP)

Intel Supervisor Mode Access Protection (SMAP) is a mechanism that provides next level of system protection by blocking a malicious user from tricking the operating system into branching off user data. This technology shuts down very popular attack vectors against operating systems.

For more information, refer to the *Intel* [®] 64 and *IA-32 Architectures Software* Developer's Manual, Volume 3A: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.9 Intel[®] Memory Protection Extensions (Intel[®] MPX)

Intel[®] MPX provides hardware accelerated mechanism for memory testing (heap and stack) buffer boundaries in order to identify buffer overflow attacks.

An $Intel^{\circledR}$ MPX enabled compiler inserts new instructions that tests memory boundaries prior to a buffer access. Other $Intel^{\circledR}$ MPX commands are used to modify a database of memory regions used by the boundary checker instructions.

The Intel $^{\mathbb{R}}$ MPX ISA is designed for backward compatibility and will be treated as no-operation instructions (NOPs) on older processors.



Intel® MPX can be used for:

- · Efficient runtime memory boundary checks for security-sensitive portions of the application.
- As part of a memory checker tool for finding difficult memory access errors. Intel[®] MPX is significantly of magnitude faster than software implementations.

Intel® MPX emulation (without hardware acceleration) is available with the Intel® C++ Compiler 13.0 or newer.

For more information, refer to the Intel® MPX documentation.

ined un 3.2.10 Intel[®] Software Guard Extensions (Intel[®] SGX)

Software Guard Extensions (SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks.

Software Guard Extensions (SGX) creates and operates in protected regions of memory named Enclaves.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code.

The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves.

Software Guard Extensions (SGX) features a memory encryption engine that both encrypt Enclave memory as well as protect it from corruption and replay attacks.

Software Guard Extensions (SGX) benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development Environment)

Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Refer to Section 3.1.2 Intel® VT-d for directed

Jefired undefined undefined undefined Datasheet, Volume 1 of 2



3.3 Power and Performance Technologies

3.3.1 Intel[®] Hyper-Threading Technology (Intel[®] HT Technology)

The processor supports Intel[®] Hyper-Threading Technology (Intel[®] HT Technology) that allows an execution processor IA core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

Intel recommends enabling Intel Hyper-Threading Technology with Microsoft* Windows* 8 and Microsoft* Windows* 7 and disabling Intel Hyper-Threading Technology using the BIOS for all previous versions of Windows* operating systems. For more information on Intel Hyper-Threading Technology, see http://www.intel.com/technology/hyper-threading/.

Note: Intel[®] HT Technology may not be available on all SKUs.

3.3.2 Intel[®] Turbo Boost Technology 2.0

The Intel[®] Turbo Boost Technology 2.0 allows the processor IA core/processor graphics core to opportunistically and automatically run faster than the processor IA core base frequency/processor graphics base frequency if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will increase the ratio of application power towards TDP and also allows to increase power above TDP as high as PL2 for short periods of time. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

3.3.2.1 Intel[®] Turbo Boost Technology 2.0 Frequency

To determine the highest performance frequency amongst active processor IA cores, the processor takes the following into consideration:

- The number of processor IA cores operating in the C0 state.
- The estimated processor IA core current consumption and I_{CCMax} register settings.
- The estimated package prior and present power consumption and turbo power limits.
- The package temperature.
- Sustained turbo residencies at high voltages and temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay within its TDP limit. Turbo processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states, see Chapter 4, "Power Management".



3.3.3 Intel[®] Advanced Vector Extensions 2 (Intel[®] AVX2)

Intel[®] Advanced Vector Extensions 2.0 (Intel[®] AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel[®] AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.

For more information on Intel AVX, see http://www.intel.com/software/avx

Intel[®] Advanced Vector Extensions (Intel[®] AVX) are designed to achieve higher throughput to certain integer and floating point operation. Due to varying processor power characteristics, utilizing AVX instructions may cause a) parts to operate below the base frequency, b) some parts with Intel[®] Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software, and system configuration and you should consult your system manufacturer for more information. Intel[®] Advanced Vector Extensions refers to Intel[®] AVX, Intel[®] AVX2, or Intel[®] AVX-512.

Note: Intel AVX2 Technology may not be available on all SKUs.

3.3.4 Intel[®] 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
 - Delivery modes
 - Interrupt and processor priorities
 - Interrupt sources
 - Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
 - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
 - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly



increased processor addressability and some enhancements on interrupt delivery.

- Increased range of processor addressability in x2APIC mode:
 - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32bits in a software transparent fashion.
 - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) 16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
 - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the
 programming of frequently-used APIC registers by system software. Specifically,
 the software semantics for using the Interrupt Command Register (ICR) and End Of
 Interrupt (EOI) registers have been modified to allow for more efficient delivery
 and dispatching of interrupts.
- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Note: Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel[®] 64 Architecture x2APIC Specification at http://www.intel.com/products/processor/manuals/.

3.3.5 Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or processor IA cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active processor IA cores without waking the deep idle processor IA cores. For performance, it routes the interrupt to the idle (C1) processor IA cores without interrupting the already heavily loaded processor IA cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

3.3.6 Intel[®] Transactional Synchronization Extensions (Intel[®] TSX-NI)

Intel[®] Transactional Synchronization Extensions (Intel[®] TSX-NI) provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the



performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX-NI may be found in $Intel^{\circledR}$ Architecture Instruction Set Extensions Programming Reference.

Note: Intel[®] TSX-NI may not be available on all SKUs.

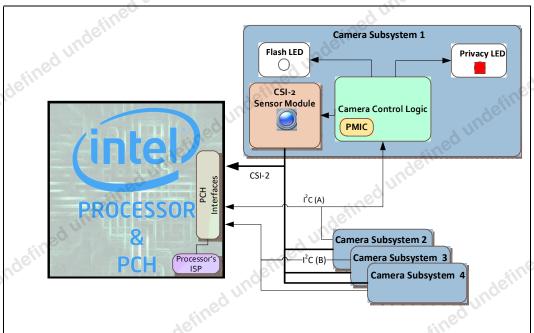
3.4 Intel[®] Image Signal Processor (Intel[®] ISP)

3.4.1 Platform Imaging Infrastructure

The imaging infrastructure is based on a number of hardware components as shown in Figure 3-3. The three major components of the system are:

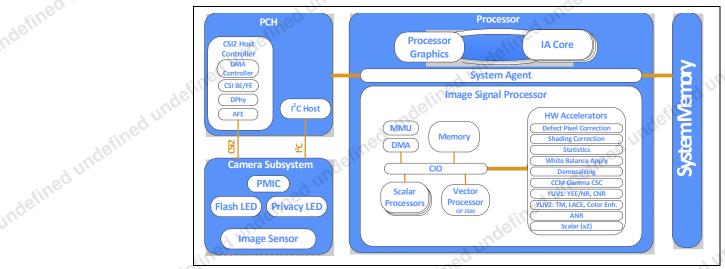
- Camera SubSystem: Located in the lid of the system and contains CMOS sensor, flash, LED, I/O interface (MIPI* CSI-2 and I²C*), Focus control and other components.
- Camera I/O controller: The I/O controller is located in the PCH and contains a MIPI-CSI2 Host controller. The host controller is a PCI device (independent of the ISP device). The CSI-2 HCI brings imaging data from an external imager into the system and provides a command and control channel for the imager using I²C.
- Intel® ISP (Image Signal Processor): The ISP processes the images captured by Bayer sensors to be used by still or video applications (such as, JPEG, H.264, and so on).

Figure 3-2. Processor Camera System





Platform Imaging Infrastructure



Debug Technologies

Intel® Processor Trace 3.5.1

Intel[®] Processor Trace (Intel[®] PT) is a new tracing capability added to Intel[®] Architecture, for use in software debug and profiling. Intel PT provides the capability for more precise software control flow and timing information, with limited impact to software execution. This provides enhanced ability to debug software crashes, hangs, or other anomalies, as well as responsiveness and short-duration performance issues.

Intel® VTune™ Amplifier for Systems and the Intel® System Debugger are part of Intel® System Studio 2015, which includes updates for new debug and trace features on this latest platform, including Intel PT and Intel® Trace Hub.

An update to the Linux perf utility, with support for Intel PT, is available for download at https://github.com/virtuoso/linux-perf/tree/intel pt. It requires rebuilding the kernel qui qui undefined undefine and the perf utility. A ati.

Jundefined undefined undefined



4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor IA Core Power Management
- Integrated Memory Controller (IMC) Power Management
- PCI Express* Power Management
- · Direct Media Interface (DMI) Power Management
- Processor Graphics Power Management



Figure 4-1. **Processor Power States**

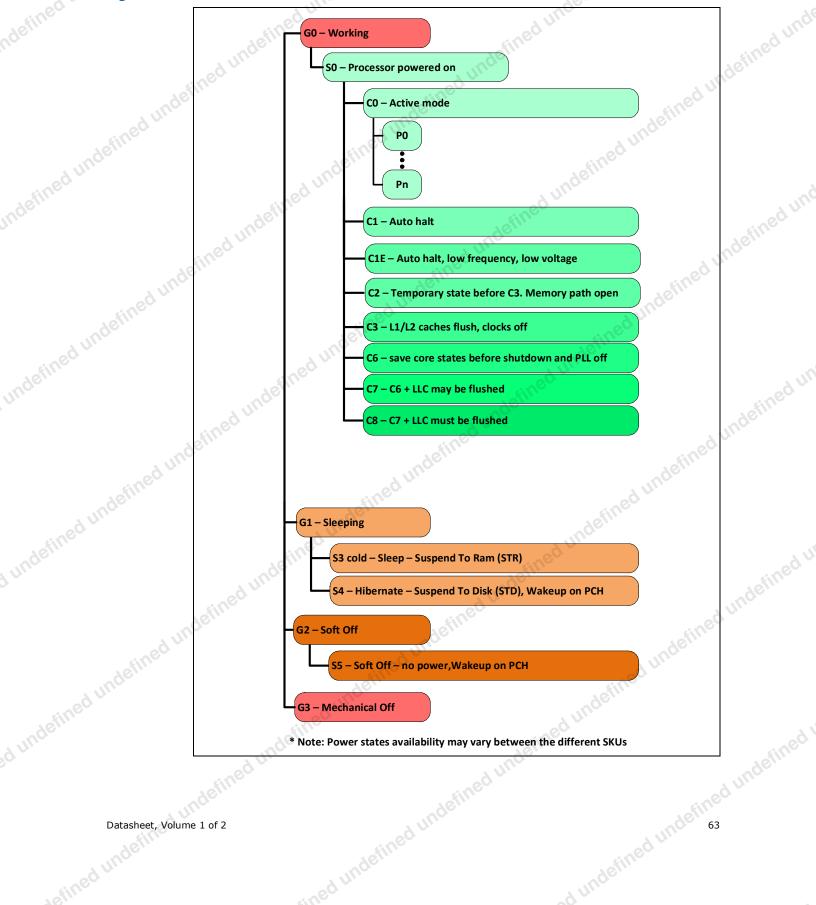
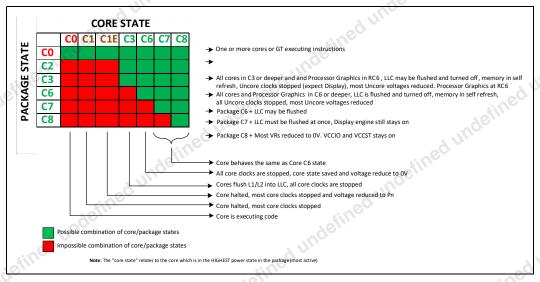




Figure 4-2. **Processor Package and IA Core C-States**



Advanced Configuration and Power Interface (ACPI) States Supported

This section describes the ACPI states supported by the processor.

System States Table 4-1.

		A SA
MUC	State	Description
	G0/S0	Full On
27.	G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
ed u.	G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).
efine	G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.
inoc	G3	Mechanical off. All power removed from system.
Jundefined undefined undef	ndefined u	Soft off. All power lost (except wake-up on PCH). Total reboot. Mechanical off. All power removed from system. Datasheet, Volume 1 of
Jundefine	ndefined i	undefined undefi
64		Datasheet Volume 1 of
ndefines		Jatasieet, volume 1 of
i chin		iner d'un



Processor IA Core/Package State Support Table 4-2.

18tine	State	Description
VO.	CO de la constantina della con	Active mode, processor executing code.
	C1	AutoHALT processor IA core state (package C0 state).
26	C1E	AutoHALT processor IA core state with lowest frequency and voltage operating point (package C0 state).
ad uno	C2	All processor IA cores in C3 or deeper. Memory path open. Temporary state before Package C3 or deeper.
define	C3	Processor IA execution cores in C3 or deeper, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache. LLC may be flushed. Clocks are shut off to each core.
ofined une	C6	Processor IA execution cores in this state save their architectural state before removing core voltage. BCLK is off.
Indefine	C7	Processor IA execution cores in this state behave similarly to the C6 state. If all execution cores request C7, LLC ways may be flushed until it is cleared. If the entire LLC is flushed, voltage will be removed from the LLC.
	C8	C7 plus LLC must be flushed.

Note: Package C-states above C8 are not supported on the S-Processor Line.

Table 4-3. Integrated Memory Controller (IMC) States

	· // /
State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 4-4. PCI Express* Link States

State	Description	defill
LO	Full on – Active transfer state.	4 1111
L1	Lowest Active Power Management – Longer exit latency	sine c
L3	Lowest power state (power-off) – Longest exit latency	vger.

Direct Media Interface (DMI) States Table 4-5.

	State	Description	
	LO	Full on – Active transfer state	65
nu ,	L1	Lowest Active Power Management – Longer exit latency	igine
ined	L3	Lowest power state (power-off) – Longest exit latency	1100
ed undefined undefined un	i efined ur	ndefined undefined undefin	
Datasheet, Volume		undeh	adefine
Battasheet, Volume	2 2 3 1 2	undefined by	defined under 65
4efineu		ined un	G.



Table 4-6. G, S, and C Interface State Combinations

Table 4-6.	G, S, ar	nd C Interfac	e State Combin	nations	"gel		
ndefine	Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description	ined und
	G0	S0	C0	Full On	On	Full On	delli
	G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt	July 1
	G0	S0	C3	Deep Sleep	On	Deep Sleep	1
defined undefined un.	G0	S0	C6/C7	Deep Power Down	On	Deep Power Down	
deili	G0	S0	C8	Off	On	Deeper Power Down	1
d Unit	G1	S3	Power off	Off	Off, except RTC	Suspend to RAM	1
	G1	S4	Power off	Off	Off, except RTC	Suspend to Disk	
deli	G2	S 5	Power off	Off	Off, except RTC	Soft Off	4 010
	G3	N/A	Power off	Off	Power off	Hard off	eined
		· U			J		1611

4.2 **Processor IA Core Power Management**

While executing code, Enhanced Intel SpeedStep® Technology and Hardware-controlled P-states optimizes the processor's IA core frequency and voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

OS/HW controlled P-states

Enhanced Intel® SpeedStep® Technology 4.2.1.1

Enhanced Intel[®] SpeedStep[®] Technology enables OS to control and select P-state. The following are the key features of Enhanced Intel[®] SpeedStep[®] Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor IA cores.
 - Once the voltage is established, the PLL locks on to the target frequency.
 - All active processor IA cores share the same frequency and voltage. In a multicore processor, the highest frequency P-state requested among all active IA cores is selected.
 - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of indefined undefined undefined undefi transitions per-second are possible.

Jefired undefined undefined un Datasheet, Volume 1 of 2



4.2.1.2 Intel[®] Speed Shift Technology

Hardware-controlled P-states are an energy efficient method of frequency control by the hardware rather than relying on OS control. OS is aware of available hardware P-states and request a desired P-state or it can let Hardware determine the P-state. The OS request is based on its workload requirements and awareness of processor capabilities. Processor decision is based on the different system constraints for example: Workload demand, thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the Operating System.

For more details, refer to the document listed below (see Related Documents section in Chapter 1, "Introduction".

• Intel® 64 and IA-32 Architectures Software Developer's Manual (SDM), volume 3B.

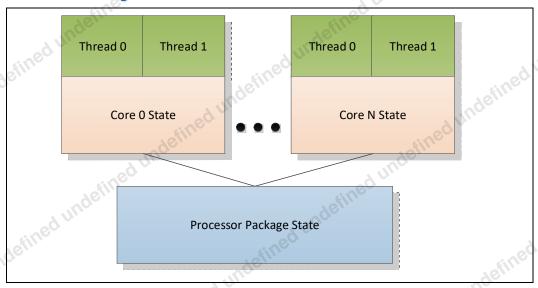
4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, deeper C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor IA core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Caution:

Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 4-3. Idle Power Management Breakdown of the Processor IA Cores



While individual threads can request low-power C-states, power saving actions only take place once the processor IA core C-state is resolved. processor IA core C-states are automatically resolved by the processor. For thread and processor IA core C-states, a transition to and from CO state is required before entering any other C-state.

Datasheet, Volume 1 of 2 Indefined under indef



4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

When P_LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wake up on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Processor IA core C-State Rules

The following are general rules for all processor IA core C-states, unless specified otherwise:

- A processor IA core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3 state, resulting in a processor IA core C1E state). See the G, S, and C Interface State Combinations table.
- A processor IA core transitions to C0 state when:
 - An interrupt occurs
 - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
 - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes up only that thread.
- If any thread in a processor IA core is active (in C0 state), the core's C-state will resolve to C0.
- Any interrupt coming into the processor package may wake any processor IA core.
- A system reset re-initializes all processor IA cores.

Processor IA core CO State

The normal operating state of a processor IA core where code is being executed.

Processor IA core C1/C1E State

C1/C1E is a low-power state entered when all threads within a processor IA core execute a HLT or MWAIT(C1/C1E) instruction.



A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel 64 and IA-32 Architectures Software Developer's Manual* for more information.

While a processor IA core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.

Processor IA core C3 State

Individual threads of a processor IA core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A processor IA core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared LLC, while maintaining its architectural state. All processor IA core clocks are stopped at this point. Because the processor IA core's caches are flushed, the processor does not wake any processor IA core that is in the C3 state when either a snoop is detected or when another processor IA core accesses cacheable memory.

Processor IA core C6 State

Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

Processor IA core C7-C10 States

Individual threads of a processor IA core can enter the C7, C8, C9, or C10 state by initiating a P_LVL4, P_LVL5, P_LVL6, P_LVL7 I/O read (respectively) to the P_BLK or by an MWAIT(C7/C8/C9/C10) instruction. The processor IA core C7-C10 state exhibits the same behavior as the processor IA core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a processor IA core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each processor IA core's immediate residency history. Upon each processor IA core C6/C7 request, the processor IA core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a processor IA core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually. If the interrupt rate experienced on a processor IA core is high and the processor IA core is rarely in a deep C-state between such interrupts, the processor IA core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a processor IA core to C1 as compared to C3.



ed undefined undefined This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 **Package C-States**

The processor supports C0, C1/C1E, C3, C6, C7, C8 power states. The following is a summary of the general rules for package C-state entry. These apply to all package Cstates, unless specified otherwise:

- A package C-state request is determined by the lowest numerical processor IA core C-state amongst all processor IA cores.
- A package C-state is automatically resolved by the processor depending on the processor IA core idle power states and the status of the platform components.
 - Each processor IA core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
 - The platform may allow additional power savings to be realized in the processor.
 - For package C-states, the processor is not required to enter C0 before entering any other C-state.
 - Entry into a package C-state may be subject to auto-demotion that is, the processor may keep the package in a deeper package C-state then requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

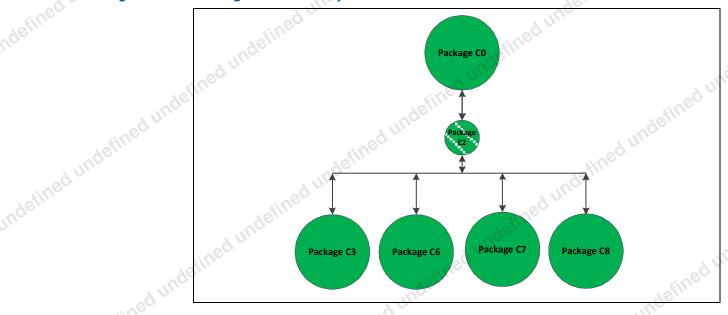
The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a processor IA core break event is received, the target processor IA core is activated and the break event message is forwarded to the target processor IA core.
 - If the break event is not masked, the target processor IA core enters the processor IA core CO state and the processor enters package CO.
 - If the break event is masked, the processor attempts to re-enter its previous package state.
- · If the break event was due to a memory access or snoop request,
 - But the platform did not request to keep the processor in a higher package Cstate, the package returns to its previous C-state.
- And the platform requests a higher power C-state, the memory access or snoop d undefined undefined undefi request is serviced and the package remains in the higher power C-state.

Jesined undefined undefine



Figure 4-4. Package C-State Entry and Exit



Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its processor IA cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual processor IA cores may be in deeper power idle states while the package is in C0 state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when either:

- All processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6, but constraints (LTR, programmed timer events in the near future, and so forth) prevent entry to any state deeper than C2 state.
- Or, all processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6 and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one processor IA core is in the C3 state.
- The other processor IA cores are in a C3 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 state or deeper state but has allowed a package C3 state.

In package C3-state, the LLC shared cache is valid.



Package C6 State

A processor enters the package C6 low-power state when:

- At least one processor IA core is in the C6 state.
- The other processor IA cores are in a C6 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a C6 package state.

In package C6 state, all processor IA cores have saved their architectural state and have had their voltages reduced to zero volts. It is possible the LLC shared cache is flushed and turned off in package C6 state.

Package C7 State

The processor enters the package C7 low-power state when all processor IA cores are in the C7 or deeper state and the operating system may request that the LLC will be flushed.

processor IA core break events are handled the same way as in package C3 or C6.

Upon exit of the package C7 state, the LLC will be partially enabled once a processor IA core wakes up if it was fully flushed, and will be fully enabled once the processor has stayed out of C7 for a preset amount of time. Power is saved since this prevents the LLC from being re-populated only to be immediately flushed again. Some VRs are reduce to 0V.

Package C8 State

The processor enters C8 states when the processor IA cores lower numerical state is C8.

The C8 state is similar to C7 state, but in addition, the LLC is flushed in a single step, Vcc and VccGT are reduced to OV. The display engine stays on.

Dynamic LLC Sizing

When all processor IA cores request C7 or deeper C-state, internal heuristics dynamically flushes the LLC. Once the processor IA cores enter a deep C-state, depending on their MWAIT sub-state request, the LLC is either gradually flushed N-ways at a time or flushed all at once. Upon the processor IA cores exiting to C0 state, the LLC is gradually expanded based on internal heuristics.



Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- Display is on or off
- Single or multiple displays
- Native or non-native resolution
- Panel Self Refresh (PSR) technology

Note:

Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State.The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state. System workload, system idle, and AC or DC power also affect the deepest possible Package Cstate.

Table 4-7. Deepest Package C-State Available

adefille	fines		S-Processor Line ^{1,2}	
	Resolution	Number of Displays	PSR Enabled	PSR Disabled
	800x600 60Hz	Single	PC8	PC8
A	1024x768 60Hz	Single	PC8	PC8
, une	1280x1024 60Hz	Single	PC8	PC8
ineo	1920x1080 60Hz	Single	PC8	PC8
defill	1920x1200 60Hz	Single	PC8	PC8
June	1920×1440 60Hz	Single	PC8	PC8
ineo	2048x1536 60Hz	Single	PC8	PC8
undefined undefined uno	2560x1600 60Hz	Single	PC8	PC8
Tille	2560x1920 60Hz	Single	PC8	PC8
	2880x1620 60Hz	Single	PC8	PC8
	2880x1800 60Hz	Single	PC8	PC8
201	3200x1800 60Hz ⁴	Single	PC8	PC6
edu	3200*2000 60Hz ⁴	Single	PC8	PC6
iefine	3840x2160 60Hz ⁴	Single	PC8	PC6
inge	4096x2160 60Hz ⁴	Single	PC8	PC6
undefined undefined un			C-state with Display OFF is Cous parameters such SW and	
Juna	ned under		dundefine	

Notes:

- All Deep states are with Display ON. The deepest C-state with Display OFF is C8.
- The deepest C-state has variance, dependent various parameters such SW and Platform devices.



4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI C-states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices (such as SODIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- · Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding control signals (CLK_P/CLK_N/CKE/ODT/CS) are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with a DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface. Each channel drives 4 CKE pins, one per rank.

The CKE is one of the power-saving means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

The processor supports four different types of power-down modes in package C0 state. The different power-down modes can be enabled through configuring PM PDWN config register. The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

- No power-down (CKE disable)
- Active power-down (APD): This mode is entered if there are open pages when
 de-asserting CKE. In this mode the open pages are retained. Power-saving in this
 mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this
 mode is fined by tXP small number of cycles. For this mode, DRAM DLL must be
 on.
- **PPD/DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL must be off.
- Precharged power-down (PPD): This mode is entered if all banks in DDR are
 precharged when de-asserting CKE. Power-saving in this mode is intermediate –
 better than APD, but less than DLL-off. Power consumption is defined by IDD2P.



Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up, all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DDL-off but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal tradeoff of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down.
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible – PPD/DLL-off with a low idle timer value.
- In high-performance systems with dense packaging (that is, tricky thermal design)
 the power-down mode should be considered in order to reduce the heating and
 avoid DDR throttling caused by the heating.

The default value that BIOS configures in PM PDWN config register is 6080 – that is, PPD/DLL-off mode with idle timer of 0x80, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCLKs that a rank is idle that causes entry to the selected power mode. As this timer is set to a shorter time the IMC will have more opportunities to put the DDR in power-down. There is no BIOS hook to set this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.



4.3.2.2 **Conditional Self-Refresh**

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Section 4.6.1.1 for more details on conditional self-refresh with Intel HD Graphics enabled.

When entering the S3 - Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor IA core flushes pending cycles and then enters SDRAM ranks that are not used by the processor graphics into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service.

Table 4-8. Targeted Memory State Conditions

emory State Conditions	inde	
Memory State with Processor Graphics	Memory State with External Graphics	21
Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.	defined
If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	nuc
Self-Refresh Mode	Self-Refresh Mode	
Memory power-down (contents lost)	Memory power-down (contents lost)	1
	Memory State with Processor Graphics Dynamic memory rank power-down based on idle conditions. If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions. Self-Refresh Mode	Memory State with Processor Graphics Dynamic memory rank power-down based on idle conditions. If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions. If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions. Self-Refresh Mode Memory State with External Graphics Dynamic memory rank power-down based on idle conditions. Self-Refresh Mode

indefined undefined un **Dynamic Power-Down**

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor IA core controller can be configured to put the devices in active powerdown (CKE de-assertion with open pages) or precharge power-down (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 **DRAM I/O Power Management**

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODT and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

istined undefined undefined Datasheet, Volume 1 of 2



DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates VDDQ for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates V_{CCIO} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.3.4 **Power Training**

BIOS MRC performing Power Training steps to reduce DDR I/O power while keeping reasonable operational margins still guaranteeing platform operation. The algorithms attempt to weaken ODT, driver strength and the related buffers parameters both on the MC and the DRAM side and find the best possible trade-off between the total I/O power and the operational margins using advanced mathematical models.

PCI Express* Power Management

- Active power management support using L1 state.
- All inputs and outputs disabled in L2/L3 Ready state.

Note: Processor PEG-PCIe interface does not support Hot-Plug.

Hot-Plug like* is only supported at Processor PEG-PCIe using Thunderbolt Device.

* Turning Thunderbolt power on and Off electrically RTD3 Like

An increase in power consumption may be observed when PCI Express* ASPM capabilities are disabled.

Direct Media Interface (DMI) Power Management

• Active power management support using L1 state.

Processor Graphics Power Management 4.6

Memory Power Savings Technologies

Intel® Rapid Memory Power Management (Intel® RMPM) 4.6.1.1

Intel® Rapid Memory Power Management (Intel® RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow undefined undefined undefined the system to remain in the deeper power states longer for memory not reserved for graphics memory. Intel® RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.



4.6.1.2 Intel[®] Smart 2D Display Technology (Intel[®] S2DDT)

Intel[®] S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel[®] S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Examples where Intel S2DDT is less effective are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Examples where Intel S2DDT is less effective are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.2 Display Power Savings Technologies

4.6.2.1 Intel® (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port

Intel[®] DRRS provides a mechanism where the monitor is placed in a slower refresh rate (the rate at which the display is updated). The system is smart enough to know that the user is not displaying either 3D or media like a movie where specific refresh rates are required. The technology is very useful in an environment such as a plane where the user is in battery mode doing E-mail, or other standard office applications. It is also useful where the user may be viewing web pages or social media sites while in battery mode.

4.6.2.2 Intel® Automatic Display Brightness

Intel[®] Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel[®] Automatic Display Brightness increases the backlight setting.

4.6.2.3 Smooth Brightness

The Smooth Brightness feature is the ability to make fine grained changes to the screen brightness. All Windows* 8 system that support brightness control are required to support Smooth Brightness control and it should be supporting 101 levels of brightness control. Apart from the Graphics driver changes, there may be few System BIOS changes required to make this feature functional.

4.6.2.4 Intel[®] Display Power Saving Technology (Intel[®] DPST) 6.0

The Intel[®] DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

 The original (input) image produced by the operating system or application is analyzed by the Intel[®] DPST subsystem. An interrupt to Intel[®] DPST software is generated whenever a meaningful change in the image attributes is detected. (A



- meaningful change is when the Intel[®] DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
- 2. Intel[®] DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
- 3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel[®] DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.6.2.5 Low-Power Single Pipe (LPSP)

Low-power single pipe is a power conservation feature that helps save power by keeping the inactive pipes powered OFF. This feature is enabled only in a single display configuration without any scaling functionalities. This feature is supported from 4th Generation Intel® Core™ processor family onwards. LPSP is achieved by keeping a single pipe enabled during eDP* only with minimal display pipeline support. This feature is panel independent and works with any eDP panel (port A) in single display mode.

4.6.3 Processor Graphics Core Power Savings Technologies

4.6.3.1 Intel[®] Graphics Dynamic Frequency

Intel[®] Turbo Boost Technology 2.0 is the ability of the processor IA cores and graphics (Graphics Dynamic Frequency) cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel[®] Graphics Dynamic Frequency is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor IA core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State. Intel[®] Graphics Dynamic Frequency requires BIOS support. Additional power and thermal budget must be available.

4.6.3.2 Intel[®] Graphics Render Standby Technology (Intel[®] GRST)

The final power savings technology from Intel happens while the system is asleep. This is another technology where the voltage is adjusted down. For RC6 the voltage is adjusted very low, or very close to zero, what may reduced power by over 1000.

4.6.3.3 Dynamic FPS (DFPS)

Dynamic FPS (DFPS) or dynamic frame-rate control is a runtime feature for improving power-efficiency for 3D workloads. Its purpose is to limit the frame-rate of full screen 3D applications without compromising on user experience. By limiting the frame rate, the load on the graphics engine is reduced, giving an opportunity to run the Processor Graphics at lower speeds, resulting in power savings. This feature works in both AC/DC modes.



4.7 Voltage Optimization

Voltage Optimization opportunistically provides reduction in power consumption; that is, a boost in performance at a given PL1. Over time the benefit is reduced. There is no change to base frequency or turbo frequency. During system validation and tuning, this feature should be disabled to reflect processor power and performance that is expected over time.

This feature is available on selected SKUs

d underined underined underined underined underined underined underined under the dunderined under the dunder the dunderined under the dunder the dund



Thermal Management

5.1 **Processor Thermal Management**

The thermal solution provides both component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel processorbased systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature (Tj_{MAX}) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skintemperatures, and exhaust-temperature requirements.

Caution:

Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP is a power dissipation and junction temperature operating condition limit, specified in this document, that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment, TDP may be exceeded for short periods of time or if running a very high power workload.

The processor integrates multiple processing IA cores and graphics cores on a single package. This may result in power distribution differences across the package and must be considered when designing the thermal solution.

Intel® Turbo Boost Technology 2.0 allows processor IA cores to run faster than the base frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery and current control limits. When Intel® Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of estimated available energy budget in the processor package.
- The processor may exceed the TDP for short durations to utilize any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Graphics peak frequency operation is based on the assumption of only one of the graphics domains (GT/GTx) being active. This definition is similar to the IA core Turbo concept, where peak turbo frequency can be achieved when only one IA core is active. Depending on the workload being applied and the distribution across the graphics domains the user may not observe peak graphics frequency for a given workload or benchmark.
- . A undefined undefined undefined Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues.

Intel® Turbo Boost Technology 2.0 availability may vary between the different SKUs. Note:



Intel® Turbo Boost Technology 2.0 Power Monitoring

When operating in turbo mode, the processor monitors its own power and adjusts the processor and graphics frequencies to maintain the average power within limits over a thermally significant time period. The processor estimates the package power for all components on package. In the event that a workload causes the temperature to exceed program temperature limits, the processor will protect itself using the Adaptive Thermal Monitor.

Intel® Turbo Boost Technology 2.0 Power Control

Illustration of Intel® Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces.

5.1.3.1 **Package Power Control**

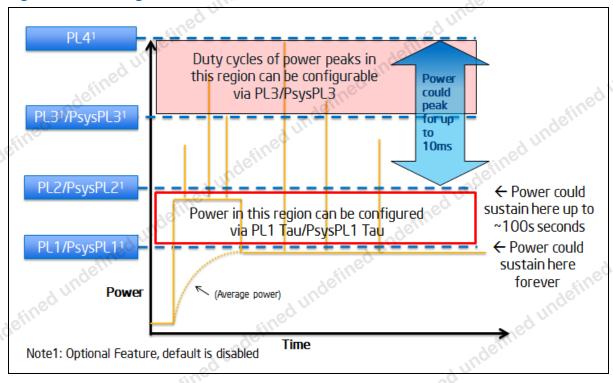
The package power control settings of PL1, PL2, PL3, PL4 and Tau allow the designer to configure Intel® Turbo Boost Technology 2.0 to match the platform power delivery and package thermal solution limitations.

- Power Limit 1 (PL1): A threshold for average power that will not exceed recommend to set to equal TDP power. PL1 should not be set higher than thermal solution cooling limits.
- Power Limit 2 (PL2): A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- Power Limit 3 (PL3): A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency. This is an optional setting.
- Power Limit 4 (PL4): A limit that will not be exceeded, the PL4 power limiting algorithms will preemptively limit frequency to prevent spikes above PL4.
- Turbo Time Parameter (Tau): An averaging constant used for PL1 exponential weighted moving average (EWMA) power calculation.

Implementation of Intel® Turbo Boost Technology 2.0 only requires configuring PL1, Note: Indefined undefined undefi PL1 Tau, and PL2.



Figure 5-1. **Package Power Control**



5.1.3.2 **Platform Power Control**

The processor introduces Psys (Platform Power) to enhance processor power management. The Psys signal needs to be sourced from a compatible charger circuit and routed to the IMVP8 (voltage regulator). This signal will provide the total thermally relevant platform power consumption (processor and rest of platform) using SVID to the processor.

When the Psys signal is properly implemented, the system designer can utilize the package power control settings of PsysPL1/Tau, PsysPL2 and PsysPL3 for additional manageability to match the platform power delivery and platform thermal solution limitations for Intel[®] Turbo Boost Technology 2.0. The operation of the PsysPL1/tau, PsysPL2 and PsysPL3 is analogous to the processor power limits described in Section 5.1.3.1.

- Platform Power Limit 1 (PsysPL1): A threshold for average platform power that will not be exceeded - recommend to set to equal platform thermal capability.
- Platform Power Limit 2 (PsysPL2): A threshold that if exceeded, the PsysPL2 rapid power limiting algorithms will attempt to limit the spikes above PsysPL2.
- Platform Power Limit 3 (PsysPL3): A threshold that if exceeded, the PsysPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL1 Tau: An averaging constant used for PsysPL1 exponential weighted moving average (EWMA) power calculation.
- . I undefined undefined The Psys signal and associated power limits/Tau are optional for the system designer and disabled by default.
- The Psys data will not include power consumption for charging.



Turbo Time Parameter (Tau) 5.1.3.3

Turbo Time Parameter (Tau) is a mathematical parameter (units of seconds) that value and/or Turbo Time Parameter is changed during runtime, may take some time based on the new Turbo Time Parameter level for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change, power limits and other factors. There is an individual Turbo Time Parameter associated with Package Power Control and Platform Power Co

Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design option where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button, cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Note: Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

5.1.4.1 **Configurable TDP**

Configurable TDP availability may vary between the different SKUs. Note:

> With cTDP, the processor is now capable of altering the maximum sustained power with an alternate processor IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

Table 5-1. **Configurable TDP Modes**

stines	cTDP consists of	f three modes as shown in the following table.	
Table 5-1.	Configurable 7	DP Modes	ined b
3	Mode	Description	deili
ined "	Base	The average power dissipation and junction temperature operating condition limit, specified in Table 5-2 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.	d uli
fined undefill	TDP-Up	The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.	
ed under	TDP-Down	The processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Down configuration in Table 5-2. The Configurable TDP-Down Frequency and corresponding TDP is lower than the processor IA core Base Frequency and SKU Segment Base TDP.	indefined !
	indefin	define	led or
84		Datasheet, Volume 1 of 2	!
sed undefills		d undefined units indefined units	
4efill		inec adult	



In each mode, the Intel[®] Turbo Boost Technology 2.0 power limits are reprogrammed along with a new OS controlled frequency range. The DPTF driver assists in all these operations. The cTDP mode does not change the max per-processor IA core turbo frequency.

5.1.4.2 **Low-Power Mode**

Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Through the DPTF driver, LPM can be configured to use each of the following methods to reduce active power:

- Restricting package power control limits and Intel[®] Turbo Boost Technology availability
- Off-Lining processor IA core activity (Move processor traffic to a subset of cores)
- Placing a processor IA Core at LFM or LSF (Lowest Supported Frequency)
- Using IA clock modulation
- LPM power as listed in Table 5-2 is defined at point which processor IA core working at LSF, GT = RPn and 1 IA core active

Off-lining processor IA core activity is the ability to dynamically scale a workload to a limited subset of cores in conjunction with a lower turbo power limit. It is one of the main vectors available to reduce active power. However, not all processor activity is ensured to be able to shift to a subset of cores. Shifting a workload to a limited subset of cores allows other processor IA cores to remain idle and save power. Therefore, when LPM is enabled, less power is consumed at equivalent frequencies.

Minimum Frequency Mode MFM of operation, which is the lowest supported frequency (LSF) at the LFM voltage, has been made available for use under LPM for further reduction in active power beyond LFM capability to enable cooler and quieter modes of operation.

undefined un5.1.5 **Thermal Management Features**

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. To protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor IA core power consumption and temperature until it operates below its maximum operating temperature. Processor IA core power reduction is achieved by:

- . I undefined undefined undefined · Adjusting the operating frequency (using the processor IA core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor IA core clocks (duty cycle).



The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS), meets its maximum operating temperature. The maximum operating temperature implies maximum junction temperature Tj_{MAX} .

Reaching the maximum operating temperature activates the Thermal Control Circuit (TCC). When activated the TCC causes both the processor IA core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE TARGET (0x1A2) MSR, bits [23:16].

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor thermal control to PL1 = TDP. The system design should provide a thermal solution that can maintain normal operation when PL1 = TDP within the intended usage range.

Adaptive Thermal Monitor protection is always enabled.

5.1.5.1.1 TCC Activation Offset

TCC Activation Offset can be set as an offset from Tj_max to lower the onset of TCC and Adaptive Thermal Monitor. In addition, the processor has added an optional time window (Tau) to manage processor performance at the TCC Activation offset value using an EWMA (Exponential Weighted Moving Average) of temperature.

TCC Activation Offset with Tau=0

An offset (degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], the offset value will be subtracted from the value found in bits [23:16]. When the time window (Tau) is set to zero, there will be no averaging, the offset, will be subtracted from the ${\rm Tj}_{\rm MAX}$ value and used as a new max temperature set point for Adaptive Thermal Monitoring. This will have the same behavior as in prior products to have TCC activation and Adaptive Thermal Monitor to occur at this lower target silicon temperature.

If enabled, the offset should be set lower than any other passive protection, such as ACPI _PSV trip points.

TCC Activation Offset with Tau

To manage the processor with the EWMA (Exponential Weighted Moving Average) of temperature, an offset (degrees Celsius) is written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], and the time window (Tau) is written to the TEMPERATURE_TARGET (0x1A2) MSR [6:0]. The Offset value will be subtracted from the value found in bits [23:16] and be the temperature.

The processor will manage to this average temperature by adjusting the frequency of the various domains. The instantaneous Tj can briefly exceed the average temperature. The magnitude and duration of the overshoot is managed by the time window value (Tau).

This averaged temperature thermal management mechanism is in addition, and not instead of Tj_{MAX} thermal management. That is, whether the TCC activation offset is 0 or not, TCC Activation will occur at Tj_{MAX} .



5.1.5.1.2 Frequency/Voltage Control

Upon Adaptive Thermal Monitor activation, the processor attempts to dynamically reduce processor temperature by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor IA core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor IA core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the processor IA core bus ratio and number of processor IA cores in deep C-states.
- The processor IA core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the trigger temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor IA core will transition to the new target automatically.

- On an upward operating point transition the voltage transition precedes the frequency transition.
- On a downward transition the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor IA core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor IA core optimized target frequency, the processor will transition to the P-state operating point.

5.1.5.1.3 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Clock modulation will not be activated by the package average temperature control mechanism.



5.1.5.2 Digital Thermal Sensor

Each processor has multiple on-die Digital Thermal Sensor (DTS) that detects the processor IA, GT and other areas of interest instantaneous temperature.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Section 2.6.

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given DTS. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE THERM STATUS MSR 1B1h and IA32 THERM STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C- states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0x0, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both processor IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the processor IA core's local APIC. Refer to the Intel 64 and IA-32 Architectures Software Developer's Manual for specific register and programming details.

5.1.5.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ± 5 °C within the entire operating range.

5.1.5.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability before the DTS reading reaches Tj_{MAX} .

5.1.5.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.



5.1.5.4 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- · Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system deasserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 μs . The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.1.5.5 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.1.5.6 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).



5.1.5.7 Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wake up, if the processor is still hot, the PROCHOT# will re-assert, although typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor IA core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.1.5.8 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point the THERMTRIP# signal will go active.

5.1.5.9 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the Intel® 64 and IA-32 Architectures Software Developer's Manual.

5.1.5.10 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.1.5.11 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to 1, the processor will immediately reduce its power consumption using modulation of the internal processor IA core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor IA core's clock independently.



I/O Emulation-Based On-Demand Mode 5.1.5.12

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor IA cores simultaneously.

Intel® Memory Thermal Management

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor, either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

Memory temperature can be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reports to the processor through the PECI 3.1 interface. This methodology is known as PECI injected temperatures, this is a method of Closed Loop Thermal Management (CLTM). CLTM requires the use of a physical thermal sensor. EXTTS# is another method of CLTM but it is only capable of reporting memory thermal status to the processor. EXTTS# consists of two GPIO pins on the PCH, where the state of the pins is communicated internally to the processor.

When a physical thermal sensor is not available to report temperature, the processor supports Open Loop Thermal Management (OLTM) that estimates the power consumed per rank of the memory using the processor's DRAM power meter. A per rank power is associated with the warm and hot thresholds that, when exceeded, may trigger memory thermal throttling.

Scenario Design Power (SDP) 5.1.7

Scenario Design Power (SDP) is a usage-based design specification, and provides additional guidance for an average power dissipation and junction temperature operating condition limit.

SDP requires that the POWER_LIMIT_1 (PL1) to be set to the cooling level capability (SDP level, or higher). While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at ${\sf Tj}_{\sf MAX}$. Customers may choose to program the TCC Offset to have TCC Activation at 80 °C, but it is not required.

The processors that have SDP specified can still exceed SDP under certain workloads such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note: cTDP-Down mode is required for Intel Core products in order to achieve SDP.

Although SDP is defined at 80 °C, the TCC activation temperature is Tj_{MAX}. Note:

. A undefined undefined undefined Datasheet, Volume 1 of 2



ned undefined undefined ndefined und 5.2 **S-Processor Line Thermal and Power Specifications**

Spe The fo	llowing notes apply to Table 5-2	red
Note	Definition	defill
undefined und 1 2 3 4	The TDP and Configurable TDP values are the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.	
adefine 2	TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications.	
3	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.	
4	'Turbo Time Parameter' is a mathematical parameter (units of seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. refer to Section 5.1.3.2 for further information.	
5	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.	define
6 7 8 9 10	Processor will be controlled to specified power limit as described in Section 5.1.2. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.	Unc
rine 7	This is a hardware default setting and not a behavioral characteristic of the part.	
8	For controllable turbo workloads, the PL2 limit may be exceeded for up to 10 ms.	
9	Refer to Table 5-1 for the definitions of 'base', 'TDP-Up' and 'TDP-Down'.	
10	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.	
11	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).	1efin
12	N/A	MOS
13	cTDP down power is based on GT2 equivalent graphics configuration. cTDP down does not decrease the number of active Processor Graphics EUs, but relies on Power Budget Management (PL1) to achieve the specified power level.	
ineo 14	May vary based on SKU.	
15	N/A	
16	Sustained residencies at high voltages and temperatures may temporarily limit turbo frequency.	
14 15 16 Indefined undefined undefin	Datasheet, Volume 1 of 2	d undefil
	defined units	
92 aned under	Datasheet, Volume 1 of 2	ed undef

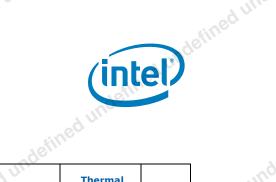


Table 5-2. TDP Specifications (S-Processor Line)

ndefinec	Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Configuration	Processor IA Core Frequency	Graphics core Frequency	Thermal Design Power (TDP) [W]	Notes
	100	Quad Core GT2 91W	Base	3.5 MHz to 4.0 GHz	350 MHz to 1.15 GHz	91	1,9,10, 11,12
4 Une	edune	9100	LPM	800 MHz	350 MHz	N/A	11,12
Indefined undefined undef		Quad Core GT2 65W	Base	2.7 MHz to 3.4 GHz	350 MHz to 1.15 GHz	65	1,9,10, 11,12
Inac		03W	LPM	800 MHz	350 MHz	N/A	11,12
		ed une	Base	2.2 MHz to 2.8 GHz	350 MHz to	35	
inger	, ci	Quad Core GT2 35W	Configurable TDP-Down/LFM	2.0 GHz to 2.6 GHz	1.1 GHz	25	1,9,10, 11,12
	4 1111		LPM	800 MHz	350 MHz	N/A	
26	inec.	Dual Core GT2 51W	Base	3.5 GHz to 3.9 GHz	350 MHz to 1.15 GHz	51	1,9,10, 11,12
IIno	Processor Line BGA	or	LPM	800 MHz	350 MHz	N/A	100
undefined undefined unde	Ellic BGA		Base	3.0 GHz to 3.3 GHz	350 MHz to	35	
4 unde		Dual Core GT2 35W	Configurable TDP-Down/LFM	2.8GHz	0.95 GHz	25	1,9, 10,11
		od u	LPM	800 MHz	350 MHz	N/A	
indeff.		Dual Core GT1 54W	Base	2.8 GHz to 3.3 GHz	350 GHz to 0.9 GHz	56	1,9, 10,11
	, 110	3444	LPM	800 MHz	350 MHz	N/A	10,11
	" USO		Base	2.9 GHz	250 1411	35	
ined und	Silli	Dual Core GT1 35W	Configurable TDP-Down/LFM	2.4 GHz	350 MHz to 0.95 GHz	25	1,9, 10,11
1 V.	1		LPM	800 MHz	350 MHz	N/A	1

Low Power and TTV Specifications (S-Processor Line) (Sheet 1 of 2)

							-
Processor IA Cores, Graphics Configuration and TDP	PCG ⁷	Max. Power Package C7 (W) ^{1,4,5}	Max. Power Package C8 (W) ^{1,4,5}	TTV TDP (W) ^{6,7}	Min. T _{CASE} (°C)	Max. TTV T _{CASE} (°C)	indefined v
Quad Core GT2 91W	2015D	11	2	91	0	63.7	nuge.
Quad Core GT2 65W	2015C	11	dell'2	65	0	70.2	
Quad Core GT1 65W	2015C	11 U	3	65	0	70.2	
Quad Core GT2 25/35W	2015B	11	2	35	6 UEC	66.1	
Dual core GT1 54W Intel [®] Pentium [®] / Celeron [®]	2015C	11	2	54	Tuge 0	65.8	ره.
Dual core GT1 54W i5/i3 Processor Lines	2015C	11	3	54	0	65.8	indefined!
e 1 of 2		, 0	indefinees			ndefine	d unos
	ان ،	ndefined U			undefined	y ur.	
4	ined.			60	Ulli		



Table 5-3. Low Power and TTV Specifications (S-Processor Line) (Sheet 2 of 2)

Processor IA Cores, Graphics Configuration and TDP	PCG ⁷	Max. Power Package C7 (W) ^{1,4,5}	Max. Power Package C8 (W) ^{1,4,5}	TTV TDP (W) ^{6,7}	Min. T _{CASE} (°C)	Max. TTV T _{CASE} (°C)
Dual Core GT2 51W	2015C	11	2 117	51	0	64.6
Dual Core GT2 35W	2015B	11	Siin 2	35	0	66.1

Notes:

- Memory configured for DDR3 1333 and populated with two DIMMs per channel.

 DMI and PCIe links are at L1 ation at DTS = 50.90 and minimum. The package C-state power is the worst case power in the system configured as follows:
 - a.
- 2.
- 3.
- 4.
- b. DMI and PCIe links are at L1

 Specification at DTS = 50 °C and minimum voltage loadline.

 Specification at DTS = 35 °C and minimum voltage loadline.

 These DTS values in Notes 2 3 are based on the TCC Activation MSR having a value of 100.

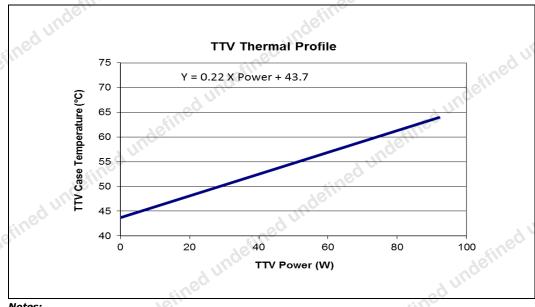
 These values are specified at VCC_MAX and VNOM for all other voltage rails for all processor frequencies. 5.
- Inese values are specified at VCC_MAX and VNOM for all other voltage rails for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static Vcc and Icc combination wherein Vccp exceeds Vccp_MAX at specified Iccp. See the loadline specifications. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at DTS = -1. TDP is achieved with the Memory configured for DDR3 1333 and 2 DIMMs per channel. Platform Compatibility Guide (PCG) (previously known as FMB) provides a design target for meeting all planted processor frequency requirements. 6.
- etin whether the street whether 7. planned processor frequency requirements. Not 100% tested. Specified by design characterization.

of the state of th



Thermal Profile for PCG 2015D Processor 5.2.1

Figure 5-2. Thermal Test Vehicle Thermal Profile for PCG 2015D Processor



Notes:

Thermal Test Vehicle Thermal Profile for PCG 2015D Processor

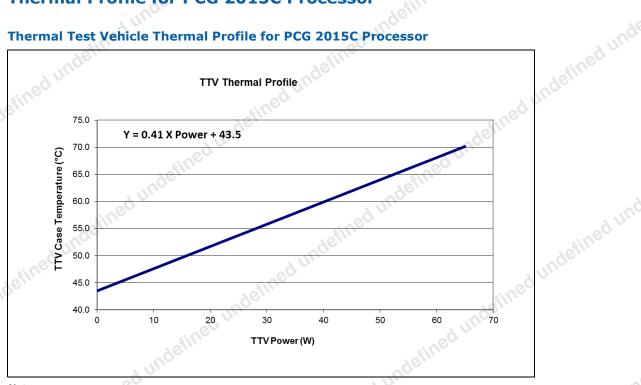
.00				1	-0
unos	Power (W)	T _{CASE_MAX} (°C)	Power (W)	T _{CASE_MAX} (°C)	undefined &
	0	43.7	46	53.8	ge,
	2	44.1	48	54.3	VILLE
d undefined undefined und	4	44.6	50	54.7	
, un	6	45.0	52	55.1	
e d	8	45.6	54	55.6	
Sille	10	45.9	56	56.0	
inde.	12	46.3	58	56.5	
A Uli	14	46.8	60	56.9	
ine.	16	47.2	62	57.3	
Aeill.	18	47.7	64	57.8	. 1/
indi	20	48.1	66	58.2	ed .
90	22	48.5	68	58.7	Silve
	24	49.0	70	59.1	undefined u
	26	49.4	72	59.5	n,
~	28	49.9	74	00.0	1
4 111	30	50.3	76	60.4	
:: DEC	32	50.7	78	60.9	
iefill.	34	51.2	80	61.3	
inol	36	51.6	82	61.7	
d undefined undefined un	38	52.1	84	62.2	
einee	40	52.5	86	62.6	
4611.	42	52.9	88	63.1	
IING	44	53.4	90	63.5	· · · · · · · · · · · · · · · · · · ·
90	46	53.8	92	63.9	
. 1/	adefined St.	Xe	ifined un.	sin ^e	d unde
	e 1 of 2	INO.		95)
Datasheet, Volume		53.8 Jundefined unde		62.6 63.1 63.5 63.9	
18/11	sin [®]		du	· · · · · · · · · · · · · · · · · · ·	

Refer to Table 5-4 for discrete points that constitute the thermal profile.



Thermal Profile for PCG 2015C Processor 5.2.2

Figure 5-3. Thermal Test Vehicle Thermal Profile for PCG 2015C Processor



Notes:

Refer to Table 5-5 for discrete points that constitute the thermal profile.

Table 5-5. Thermal Test Vehicle Thermal Profile for PCG 2015C Processor

Jundefined undefined u	Power (W)	T _{CASE_MAX} (°C)	Power (W)
, 0	0	43.5	34
rea	2	44.3	36
Jefill.	4	45.1	38
inole	6	46.0	40
	8	46.8	42
	10	47.6	44
ade.	12	48.4	46
	14	49.2	48
	16	50.1	50
	18	50.9	52
	20	51.7	53
	22	52.5	54
ineo.	24	53.3	56
46411.	26	54.2	58
1100	28	55.0	60
	30	55.8	62
	32	56.6	64
ade,	34	57.4	65
Jundefined undefined	indefined unos	57.4	Jefined under
96 undefined		undefined un	
16fine			

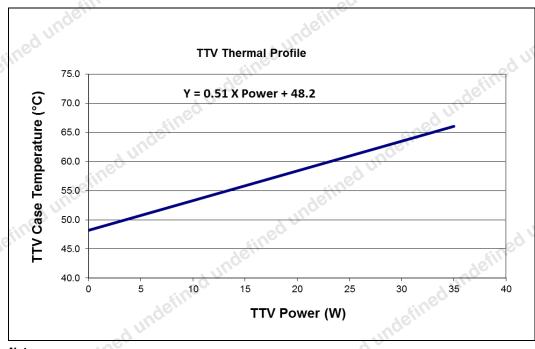
Power (W)	T _{CASE_MAX} (°C)	70.
34	57.4	
36	58.3	
38	59.1	
40	59.9	
42	60.7	
44	61.5	
46	62.4	d undefined u
48	63.2	eine -
50	64.0	gen
52	64.8	un
53	65.2	O
54	65.6	
56	66.5	
58	67.3	
60	68.1	
62	68.9	
64	69.7	
65	70.2	.6
efined under	1	ed undefined
efill	efil	

Datasheet, Volume 1 of 2 -4 undefined



5.2.3 Thermal Profile for PCG 2015B Processor

Figure 5-4. Thermal Test Vehicle Thermal Profile for PCG 2015B Processor



Notes:

Table 5-6. Thermal Test Vehicle Thermal Profile for PCG 2015B Processor

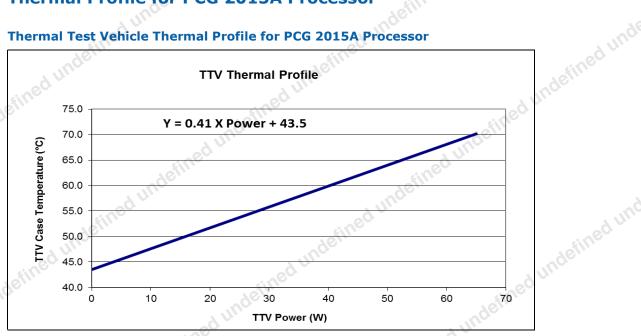
Power (W)	T _{CASE_MAX} (°C)	Power (W)	T _{CASE_MAX} (°C)
0	48.2	20	58.4
2	49.2	22	59.4
4	50.2	24	60.4
6	51.3	26	61.5
8	52.3	28	62.5
10	53.3	30	63.5
12	54.3	32	64.5
14	55.3	34	65.5
16	56.4	35	66.1
18	57.4		file

^{1.} Refer to Table 5-6 for discrete points that constitute the thermal profile.



Thermal Profile for PCG 2015A Processor 5.2.4

Thermal Test Vehicle Thermal Profile for PCG 2015A Processor Figure 5-5.



Notes:

Thermal Test Vehicle Thermal Profile for PCG 2015A Processor

unde	Power (W)	T _{CASE_MAX} (°C)	Power (W)
	0	43.5	34
	2	44.3	36
	4	45.1	38
dui	6	46.0	40
File	8	46.8	42
nder	10	47.6	44
ad uli	12	48.4	46
Stines	14	49.2	48
Jundefined undefined und	16	50.1	50
3 0.	18	50.9	52
	20	51.7	54
	22	52.5	56
10.	24	53.3	58
ined	26	54.2	60
deill	28	55.0	62
4 Unc	30	55.8	64
"ineo	32	56.6	65
ed undefined und	ndefined undefin	56.6 sined und	efined undefined s
defined undefines		led undefined by	a)

T _{CASE_MAX} (°C)
57.4
58.3
59.1
59.9
60.7
61.5
62.4
63.2
64.0
64.8
65.6
66.5
67.3
68.1
68.9
69.7
70.2

Datasheet, Volume 1 of 2 indefined.

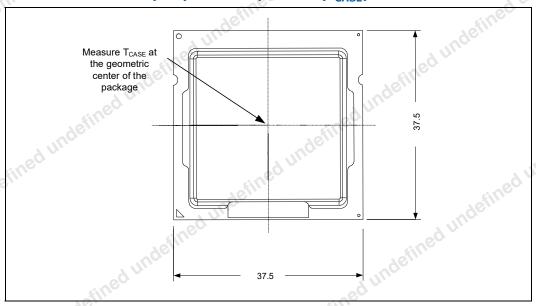
^{1.} Refer to Table 5-7 for discrete points that constitute the thermal profile.



5.2.5 Thermal Metrology

The maximum TTV case temperatures (T_{CASF-MAX}) can be derived from the data in the appropriate TTV thermal profile earlier in this chapter. The TTV T_{CASE} is measured at the geometric top center of the TTV integrated heat spreader (IHS). Figure 5-6 illustrates the location where T_{CASE} temperature measurements should be made.

Thermal Test Vehicle (TTV) Case Temperature (T_{CASE}) Measurement Location Figure 5-6.



the tollowing supplier is listed as a convenience to Intel's general customers and may be subject to change without notice. THERM-X OF CALIFORNIA, 3200 Investment Blvd, Hayward, Ca 94544. George Landis +1-510-441-7566 Ext. 368 george@therm-x com The vendor part number is XTMS1565.



6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The notations in the following table are used to describe the signal type.

The signal description also includes the type of buffer used for the particular signal (see the following table).

Table 6-1. Signal Tables Terminology

Notation	Signal Type
I	Input pin
0 100	Output pin
I/O	Bi-directional Input/Output pin
SE	Single Ended Link
Diff	Differential Link
CMOS	CMOS buffers. 1.05V- tolerant
OD	Open Drain buffer
DDR3L/-RS	DDR3L/DDR3L-RS buffers: 1.35V-tolerant
DDR4	DDR4 buffers: 1.2V-tolerant
Α	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Availability	Signal Availability condition - based on segment, SKU, platform type or any other factor
Asynchronous ¹	Signal has no timing relationship with any reference clock.
Note: 1. Qualifier for a b	puffer type.



Table 6-2.

Signal Description	ined "). ·			(intel
ined unos	dundein				Title
_	m Memory Interface		4 117	defin	
Table 6-2. DDR3L/-	RS Memory Interface (Sheet 1 of Description	of 2)	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	Data Buses: Data signals interface to the SDRAM data buses.	I/O	DDR3L	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR3L	Diff	S-Processor Line (Desktop)
DDR0_CKN[3:0] DDR0_CKP[3:0] DDR1_CKN[3:0] DDR1_CKP[3:0]	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN /DDR1_CKN are used to sample the command and control signals on the SDRAM.	o	DDR3L	Diff	S-Processor Line
DDR0_CKE[3:0] DDR1_CKE[3:0]	Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up. Power-down SDRAM ranks. Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	0	DDR3L	SE	S-Processor Line
DDR0_CS#[3:0] DDR1_CS#[3:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	DDR3L	SE	S-Processor Line
DDR0_ODT[3:0] DDR1_ODT[3:0]	On Die Termination: (1 per rank). Active SDRAM Termination Control.	0	DDR3L	SE	S-Processor Line
DDR0_MA[15:0] DDR1_MA[15:0]	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM. • A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge. • A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH: no burst chop; LOW: burst chopped.	0	DDR3L	SE	All Processor Lines
DDR0_BA[2:0] DDR1_BA[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	0	DDR3L	SE	All Processor Lines
DDR0_CAS# DDR1_CAS#	CAS Control Signal: Column Address Select command signal	0	DDR3L	SE	All Processor Lines
DDR0_RAS# DDR1_RAS#	RAS Control Signal: Row Address Select command signal	0	DDR3L	SE	All Processor Lines
Datasheet, Volume 1 of 2	fined undefil				All Processor Lines



ed undefined undefined

2	intel/	De Manary Intilized undefine	of 2)			Signal Description	
fined uni	Signal Name	-RS Memory Interface (Sheet 2 Description	Dir.	Buffer Type	Link Type	Availability	.<
	DDR0_WE# DDR1_WE#	WE Control Signal: Write Enable command signal	0	DDR3L	SE	All Processor Lines	ined u
	DDR0_VREF_DQ DDR1_VREF_DQ	Memory Reference Voltage for DQ:	0	А	SE	All Processor Lines	luge,
	DDR_VREF_CA	Memory Reference Voltage for Command & Address:	0	А	SE	All Processor Lines	
ed un	DDR_VTT_CNTL	System Memory Power Gate Control: When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and S3.	0	DDR3L	SE	All Processor Lines	
IIIE	Table 6-3. DDR4 Mg	emory Interface (Sheet 1 of 2)		defined	Jin		slined "

DDR4 Memory Interface (Sheet 1 of 2) Table 6-3.

		T	V 177.	1		T	1.00
	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	
	DDR0_DQ[63:0] DDR1_DQ[63:0]	Data Buses: Data signals interface to the SDRAM data buses.	I/O	DDR4	SE	All Processor Lines	
sined ur	DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4	Diff	S-Processor Line (Desktop)	
under	DDR0_CKN[3:0] DDR0_CKP[3:0] DDR1_CKN[3:0] DDR1_CKP[3:0]	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN /DDR1_CKN are used to sample the command and control signals on the SDRAM.	0,1	DDR4	Diff	S-Processor Line	undefinedun
undefined i	DDR0_CKE[3:0] DDR1_CKE[3:0]	Clock Enable: (1 per rank). These signals are used to: Initialize the SDRAMs during power-up. Power-down SDRAM ranks. Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	0	DDR4	SE	S-Processor Line	
4 muger	DDR0_CS#[3:0] DDR1_CS#[3:0]	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	0	DDR4	SE	S-Processor Line	d undefined ur
	DDR0_ODT[3:0] DDR1_ODT[3:0]	On Die Termination: (1 per rank). Active SDRAM Termination Control.	0	DDR4	SE	S-Processor Line	9 nue
ad undefined	undefined un	d undefined unos				defined under	
ed undefili	Leftine	SDRAM Termination Control.	ned	undefin	sq m.		ed undefined i
	102 ed unae	, undef			[Datasheet, Volume 1 of 2	60
. zeć	Jundefine	d undefined				idefined ur.	
76/11.		cine			29 n	•	



red undefined undefineu DDR4 Memory Interface (Sheet 2 of 2) Table 6-3.

fined .	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	
	, uni	Address: These signals are used to provide the multiplexed row and column address to the SDRAM.	ndef	Inec			defined ur
efined und	DDR0_MA[16:0] DDR1_MA[16:0]	 A[16:14] use also as command signals, see ACT# signal description. A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. 	0	DDR4	SE	All Processor Lines	ined l
	, undefined un	A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH, no burst chop; LOW: burst chopped).	Unde			ofined v	ndefill
tefined und	DDR0_ACT# DDR1_ACT#	Activation Command: ACT# HIGH along with CS# determines that the signals addresses below have command functionality. A16 use as RAS# signal A15 use as CAS# signal A14 use as WE# signal	0	DDR4	SE	All Processor Lines	
	DDR0_BG[1:0] DDR1_BG[1:0]	Bank Group: BG[0:1] define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.	UO IC	DDR4	SE	All Processor Lines x8 DRAM device use BG[1:0], x16 use only BG[0].	Indefined
	DDR0_BA[1:0] DDR1_BA[1:0]	Bank Address: BA[1:0] define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	0	DDR4	SE	All Processor Lines	
defined ur	DDR0_ALERT# DDR1_ALERT#	Alert: This signal is used at command training only. It is getting the Command and Address Parity error flag during training. CRC feature is not supported.	I	DDR4	SE	All Processor Lines	
<i>y</i> -	DDR0_PAR DDR1_PAR	Command and Address Parity: These signals are used for parity check.	0	DDR4	SE	All Processor Lines	indefined
	DDR_VREF_CA	Memory Reference Voltage for Command & Address:	90	А	SE	All Processor Lines	Uno
A.*	DDR_VTT_CNTL	System Memory Power Gate Control: When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and S3.	0	DDR4	SE	All Processor Lines	
isfined u		ined und		۸	und	31.	
ndefined u	ined	memory VTT regulator in C8 and S3.	ad U	ndefined		Jefined unde 103	undefine
		adefin				Stine	
refined l	Datasheet, Volume 1 of 2	defined un				sined und 103	
ined.		ed riur			, un	Je.	



PCI Express* Graphics (PEG) Signals

PCI Express* Interface **Table 6-4.**

VO.							
	Signal Nam	ie dur	Description	Dir.	Buffer Type	Link Type	Availability
	PEG_RCOMP		Resistance Compensation for PCI Express channels PEG and DMI.	N/A	Α	SE	ed
	PEG_RXP[15:0] PEG_RXN[15:0]		PCI Express Receive Differential Pairs.	I	PCI Express*	Diff	S-Processor Line
711	PEG_TXP[15:0] PEG_TXN[15:0]		PCI Express Transmit Differential Pairs.	0	PCI Express*	Diff	lued n.
defined			fined und		ed	iuge,	
	6.3 D	irect	Media Interface (DM	I) S	Signal	S	

Direct Media Interface (DMI) Signals DMI Interface Signals 6.3

DMI Interface Signals

	Signal Name	Description	Dir.	Buffer Type	Link Type		
ال لم	DMI_RXP[3:0] DMI_RXN[3:0]	DMI Input from PCH: Direct Media Interface receive differential pairs. DMI Output to PCH: Direct Media Interface transmit differential pairs.	I	DMI	Diff	S-Processor Line	
undefined u	DMI_TXP[3:0] DMI_TXN[3:0]	DMI Output to PCH: Direct Media Interface transmit differential pairs.	0	DMI	Diff	3 Frocessor Line	, ur
nuc		under		defilme		•	Lefined
	Hin	50	eq m				dunde
	d unde	indefill				define	
		ined u.				ed nuo	
001		Indell				lefine	
define					d un		47
d une		unde.		odefille			lefined
	i efil		Jed n				ed unoc
	ad unde	indeh				defin	
	definee					ed une	
d		, under				define	
adefine		is fine o			sq ni,		λ.
ed ull		d unde		"ugetill			defined
	46/	iver e	ined,				od uno
	104 ad unos	undel				Datasheet Volume 1 of	2
	define					batasheet, volume 1 of	_
o.C	June	, under				define	
4efine		ineo.			ad u		



Reset and Miscellaneous Signals

Reset and Miscellaneous Signals Table 6-6.

Signal Descript	tion	afine				(Inte
ed un		" unde				a effir
6.4	Docat	and Missallaneous S	ian-	alc		sq m.
6.4	Reset	and Miscellaneous S	iyila	115	reliu,	
Table 6-6.	Reset an	d Miscellaneous Signals		ned un		,
Signal I	Name Un	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	efined ur	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Intel recommends placing test points on the board for CFG pins. • CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall. • CFG[1]: Reserved configuration lane. • CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. - 1 = Normal operation - 0 = Lane numbers reversed. • CFG[3]: Reserved configuration lane. • CFG[4]: eDP enable: - 1 = Disabled. - 0 = Enabled. • 0 = Enabled. • 0 = Tx8, 2 x4 PCI Express* - 01 = reserved - 10 = 2 x8 PCI Express* - 11 = 1 x16 PCI Express* • CFG[7]: PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for	unde i	GTL	defil	All Processor Line
	efined	training. • CFG[19:8]: Reserved configuration lanes.	Ull			
CFG_RCOMP	O	Configuration Resistance Compensation	N/A	N/A	SE	All Processor Line
PROC_SELECT#	‡	Platform Reset pin driven by the PCH. Processor Select: This pin is for compatibility with future platforms. It should	I	CMOS	SE N/A	S-Processor Line All Processor Line
DDOC TOTOTAL		be unconnected for the processor.		CMCC	CF.	C Drawn !:
PROC_TRIGIN	г	Debug pin.	I	CMOS	SE SE	S-Processor Line
PROC_TRIGIN PROC_TRIGOUT PROC_AUDIO_S		Processor Audio Serial Data Input: This signal is an input to the processor from the	I	CMOS	SE	S-Processor Line
PROC_AUDIO_S	SDO MINEÒ	PCH. Processor Audio Serial Data Output: This signal is an output from the processor to the PCH.	9910	AUD	SE	S-Processor Line
1	101.	wale ren.	4		1	1
PROC_AUDIO_C	CLK	Processor Audio Clock	I	AUD	SE	
PROC_AUDIO_C	odefined	Processor Audio Clock	I I	AUD	SE	afined under
PROC_AUDIO_C	me 1 of 2	Processor Audio Serial Data Output: This signal is an output from the processor to the PCH. Processor Audio Clock	I I	AUD	SE	efined under

I. r. defined undefined undefined Datasheet, Volume 1 of 2 ired undefi



embedded DisplayPort* (eDP*) Signals

Table 6-7. embedded DisplayPort* Signals

	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
	eDP_TXP[3:0] eDP_TXN[3:0]	embedded DisplayPort Transmit: differential pair	0	eDP	Diff	All Processor Lines
	eDP_AUXP eDP_AUXN	embedded DisplayPort Auxiliary: Half- duplex, bidirectional channel consist of one differential pair.	0	eDP	Diff	All Processor Lines
indefined un	eDP_DISP_UTIL	embedded DisplayPort Utility: Output control signal used for brightness correction of embedded LCD displays with backlight modulation. This pin will co-exist with functionality similar to existing BKLTCTL pin on PCH	0	Async CMOS	SE	All Processor Lines
o.	eDP_RCOMP	DDI IO Compensation resistor, supporting DP*, eDP* and HDMI* channels.	N/A	А	SE	All Processor Lines

Note:

- When using eDP* bifurcation:
 x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
 x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])

Display Interface Signals 6.6

Table 6-8. Display Interface Signals

	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	, U.
undefined l	DDI1_TXP[3:0] DDI1_TXN[3:0] DDI2_TXP[3:0] DDI2_TXN[3:0] DDI3_TXP[3:0] DDI3_TXN[3:0]	Digital Display Interface Transmit: Differential Pairs	0	DP/HDMI*	Diff	All Processor Lines. DDI3_TXP[3:0] DDI3_TXN[3:0] DDI3_AUXP	. 14
J.	DDI2_AUXP DDI2_AUXN DDI3_AUXP	Digital Display Interface Display Port Auxiliary: Half-duplex, bidirectional channel consist of one differential pair for each channel.	01	DP/HDMI*	Diff	DDI3_AUXN are present in S-Processor Line.	d undefined b
d undefined	undefined	ed undefined und			4 Un	defined under	
ed under	undefine	d undefili.	ined	undefine			ed undefined i
i efined	106	d undefined undefined undefi			م الا	Datasheet, Volume 1 of 2	



Table 6-9.

	Signal Description	ined u	Wor			(inte
	ined unde	ed under.				une fill
red und		essor Clocking Signals	5	nu .	defin	
	Table 6-9. Process	or Clocking Signals		ueq.	1	1
				Descen		
	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
	Signal Name BCLKP BCLKN	Description 100 MHz Differential bus clock input to the processor	Dir.			Availability
	BCLKP	100 MHz Differential bus clock input to the	100		Туре	Availability S-Processor Line
uni	BCLKP BCLKN CLK24P	100 MHz Differential bus clock input to the processor 24 MHz Differential bus clock input to the	I		Type Diff	of ine

Testability Signals 6.8

Table 6-10. Testability Signals

	Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
undefined und	BPM#[3:0]	Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	All Processor Lines
	PROC_PRDY#	Probe Mode Ready: PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	0	OD	SE	All Processor Lines
	PROC_PREQ#	Probe Mode Request: PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	All Processor Lines
d undefined un	PROC_TCK	Test Clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal must be driven low or allowed to float during power on Reset.	I	GTL	SE	All Processor Lines
	PROC_TDI	Test Data In: This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	All Processor Lines
	PROC_TDO	Test Data Out: This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	0 0	OD	SE	All Processor Lines
	PROC_TMS	Test Mode Select: A JTAG specification support signal used by debug tools.	I	GTL	SE	All Processor Lines
	PROC_TRST#	Test Reset: Resets the Test Access Port (TAP) logic. This signal must be driven low during power on Reset.	I	GTL	SE	All Processor Lines



Error and Thermal Protection Signals

Table 6-11. Error and Thermal Protection Signals

Table 6-11. Error and	Thermal Protection Signals Description	Dir.	Buffer	Link	Availabi
CATERR#	Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	0	OD	SE	All Processor
PECI	Platform Environment Control Interface: A serial sideband interface to the processor. It is used primarily for thermal, power, and error management.	I/O	PECI, Async	SE	All Processor
PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All Processor
	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	9,17	OD	SE	All Processor I
J undefined U.	dun			d und	efined ur
fined	undefill	ed u	ndefine		
lefined under	ined undefil				ed ur
undefined undefined	undefined undefined undefined undefined undefined undefined undefined undefined undefined undefi		efin	ed un	
ed	In.	.ed.	illor		

undefined undefi



6.10

Table 6-12. Power Sequencing Signals

	indefine		1efil	led.		
Signal Description	ed u.	adefined ur				(inte
	Power Sequen			dun	defin	ed une
Signal Nar	- de//	escription	Dir.	Buffer Type	Link Type	Availability
PROCPWRGD	requires this input indication that the supplies are stable This requirement a S-state of the proof the signal will remale akage current), time that the power until they come wi	r Good: The processor signal to be a clean V_{CC} and V_{DDQ} power and within specifications. applies regardless of the cessor. 'Clean' implies that ain low (capable of sinking without glitches, from the er supplies are turned on thin specification. The ransition monotonically to	I	CMOS	SE	All Processor Lines
VCCST_PWRGD	requires this input indication that the supplies are stable This signal must h both S0 and S3 po that the signal will sinking leakage cu from the time that turned on until the	signal must then transition	I	CMOS	SE	All Processor Lines
PROC_DETECT#/SI	Pulled down direct processor package no connection to this signal. System	t/Socket Occupied: ly (0 Ohms) on the to the ground. There is he processor silicon for a board designers may use rmine if the processor is	N/A	N/A	SE	All Processor Lines
VIDSOUT VIDSCK VIDALERT#	signals comprise a synchronous interf power manageme	CK, VIDALERT#: These three-signal serial face used to transfer in information between the voltage regulator	I/O O I	OD (open drain)	SE	All Processor Lines
PM_SYNC PM_DOWN	signal to communi status from the PC	cent Sync: A sideband cate power management CH to the processor. PCH ENT# status to the	I	CMOS	SE	S-Processor Line
	PCH. Indicates pro	nent Down: Sideband to occasor wake up event The processor combines the OLTM/CLTM.	900	CMOS	SE	S-Processor Line
d undefined und	the pin status into	The processor combines the OLTM/CLTM.	ed un	defined	und	efined undefi
Datasheet, Volume	1 of 2	Indefined under				Jefined undef
,-	ined !	T.			9 nu,	

Datasheet, Volume 1 of 2 i chined undefi



Table 6-13. Processor Power Rails Signals

(intel [®])	ndefined					
sine					fills	
£///*	d un				"uge,	
6 11 Dres	essor Power Rails				ed or	
6.11 Proce	essor Power Rails				File	
	ed un			nuo		
Table 6-13. Process	or Power Rails Signals		ined			-
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability	10
Vcc	Processor IA cores power rail	I	Power	-	All Processor Lines	NO
Vcc _{GT}	Processor Graphics power rail	I	Power	-	All Processor Lines	
V _{DDQ}	System Memory power rail	I	Power	-	All Processor Lines	
VCC _{SA}	Processor System Agent power rail	I	Power	-	All Processor Lines	
NO TOTAL					::0e0	
Vcc _{IO}	Processor I/O power rail.Consists of V_{CCIO} and V_{CCIO} DDR. V_{CCIO} and V_{CCIO} should be isolated from each other.	I	Power	- 6	All Processor Lines	
Vec	Sustain voltage for processor standby	I	Dower	July Control	All Processor Lines	
Vcc _{ST}	modes		Power	-		
Vcc _{PLL}	Processor PLLs power rails	I	Power	-	All Processor Lines	۵(
Vcc _{PLL_OC}	Processor PLLs power rails	1	Power	-	All Processor Lines	n_{O}
Vcc_SENSE Vss_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure				All Processor Lines	
Vcc _{GT} _SENSE	voltage near the silicon.					
Vss _{GT} _SENSE	and of	N/A	Power	_	All Processor Lines	
Vcc _{IO} _SENSE	defill	IN/A	rowei		All Processor Lines	
Vss _{IO} _SENSE	- uno				(e)	
Vcc _{SA} _SENSE Vss _{SA} _SENSE	ineo.			4 nn.	All Processor Lines	
	Aciti:		6/17/2			J
Jundefined undefine	Jundefined undefined undef	ned "	indefin	ed ur	idefined undefine	id ur
d undefine	ed undefined und	ined	undefi	ned l'	indefined une	edv



Ground, Reserved and Non-Critical to Function (NCTF) Signals

The following are the general types of reserved (RSVD) signals and connection quidelines:

- RSVD these signals should not be connected
- RSVD_TP these signals should be routed to a test point
- RSVD NCTF these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Table 6-14.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground the resistor can also be used for system testability.

Table 6-14. GND, RSVD, and NCTF Signals

Signal Name	Description
Vss	Processor ground node
Vss_NCTF	Non-Critical To Function: These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	Reserved: All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

Processor Internal Pull-Up/Pull-Down **Terminations**

Table 6-15. Processor Internal Pull-Up/Pull-Down Terminations

indefine	Signal Name	Pull Up/Pull Down	Rail	Value
	BPM[3:0]	Pull Up	Vcc _{IO}	16-60 Ω
	PREQ#	Pull Up	Vcc _{ST}	3 kΩ
	PROC_TDI	Pull Up	Vcc _{STG} ¹	3 kΩ
	PROC_TMS	Pull Up	Vcc _{SGT} 1	3 kΩ
40	PROC_TRST#	Pull Down	-	3 kΩ
	CFG[19:0]	Pull Up	Vcc _{IO}	3 kΩ
unden	Notes: 1. For S-Processor Line,	it should be Vcc _{ST}		li)
undefined undefined t		d um	§	ed nude.
und	, under		def	ILLO
			dulle	



Electrical Specifications med under

7.1 **Processor Power Rails**

Processor Power Rails Table 7-1. •

	offined W.	ned unac		d und
L Pr	ocessor Power Rails	d undefil.		ndefinec
7 111.	cessor Power Rails	inec	"defined	7
Power Rail	Description	Control	Availability	
V _{CC}	Processor IA Cores Power Rail	SVID	All Processor Lines	
Vcc _{GT}	Processor Graphics Power Rails	SVID	All Processor Lines	
Vcc _{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	All Processor Lines	
Vcc _{IO}	IO Power Rail	Fixed	All Processor Lines	4 UIT
Vcc _{ST}	Sustain Power Rail	Fixed	All Processor Lines	"inec
Vcc _{PLL}	Processor PLLs power Rail	Fixed	All Processor Lines	oger.
Vcc _{PLL_OC} Note 1	Processor PLLs OC power Rail	Fixed	All Processor Lines	Ulli
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	All Processor Lines	
0.9				

Notes:

Power and Ground Pins 7.1.1

All power pins must be connected to their respective processor power planes, while all VSS pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop.

V_{CC} Voltage Identification (VID)

Intel processors/chipsets are individually calibrated in the factory to operate on a specific voltage/frequency and operating-condition curve specified for that individual processor. In normal operation, the processor autonomously issues voltage control requests according to this calibrated curve using the serial voltage-identifier (SVID) interface. Altering the voltage applied at the processor/chipset causing operation outside of this calibrated curve is considered out-of-specification operation.

The SVID bus consists of three open-drain signals: clock, data, and alert# to both set voltage-levels and gather telemetry data from the voltage regulators. Voltages are controlled per an 8-bit integer value, called a VID, that maps to an analog voltage level. An offset field also exists that allows altering the VID table. Alert can be used to inform the processor that a voltage-change request has been completed or to interrupt the processor with a fault notification.

For VID coding and further details, refer to the IMVP8 PWM Specification.

Jefined undefined undefined un Datasheet, Volume 1 of 2

 $^{^{\}circ}$ VCC $_{
m PLL,\,OC}$ power rail should be sourced from the VDDQ VR. The connection can be direct or through a load switch, depending desired power optimization. In case of direct connection (VCC_{PLL_OC} is shorted to VDDQ, no load switch), platform should ensure that VCC_{ST} is ON (high) while VCC_{PLL_OC} is ON (high). VCC_{STG} power rail should be sourced from the VR as VCC_{ST} . The connection can be direct or through a load switch, depending desired power optimization.



DC Specifications

The processor DC specifications in this section are defined at the processor signal pins, unless noted otherwise.

- The DC specifications for the DDR3L/-RS/DDR4 signals are listed in the Voltage and Current Specifications section.
- The Voltage and Current Specifications section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

Processor Power Rails DC Specifications

Vcc DC Specifications 7.2.1.1

Processor IA Core (Vcc) Active and Idle Mode DC Voltage and Current **Table 7-2. Specifications (Sheet 1 of 2)**

Γ			_	6			1		1
	Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Note ¹]
undefined u	Operating Voltage	Voltage Range for Processor Active Operating Mode	All undefine	0.55	_	1.52 fined w	V	1,2,3, 7,12	711
	Idle Voltage	Voltage Range for Processor Idle Mode (Package C6/ C7)	ed underta	0	-fine	undefille 0.55	v	1,2,3,	lueg r
		7 0110	S(35W)-dual core GT _{2/1}	1	96-	40			
		,O.	S(51W)-dual core GT ₂	977	_	45			
d undefined (iuq ₆₁₁ .		S(51W) - dual core GT ₁ Pentium [®] /Celeron [®]	_	_	45			
" ned			S(54W) - dual core GT ₁	_	_	58			
indefil.	I _{CCMAX}	Maximum Processor IA	S(54W) - dual core GT ₁ Pentium [®] /Celeron [®]	-	_	58	A	4,6,7, 11	ed u
9 0.	CCITO	Core I _{CC}	S(25W) - quad core GT _{2/0}	1	_	55		11	ALCO .
		25.1	S(35W) - quad core GT ₂	I	ı	66		'IUO'	
		deli	S(45W)-quad core GT ₀		70	- CO			
		red une	S(65W)-quad core GT ₀	-	1918.	79	elilli		
			S(80W) - quad core GT _{2/0}			82			
	ge,,,		S(95W)-quad core GT ₂ K-SKU	-	-	100			
A	TOB _{VCC}	Voltage Tolerance	PS0, PS1	-	_	±20	mV	3, 6, 8	
einec.	102000	Tolerance	PS2, PS3	I	-	±20			
ed undefined	Datashee	et Volume 1 of	ined undefine		Indefin	ed undefined undefined unde	5fine		Jefined 1
	Datasilee	c, volume 10	_			4 Une	113	,	
e ci	undefi		undefi	ILIA		od undefined unde			
1efine			eineo.			ad uli.			



ed undefined undefined Processor IA Core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

defined h	Symbol	Parameter	Segment	Min.	Тур.		Max.		Unit	Note
		Ripple	96,11			$I_L \leq 0.5$	0.5 <i<sub>L<i<sub>CCTDC</i<sub></i<sub>	$I_{CCTDC} < I_{L} < IccMax$		
		Tolerance	PS0	_	-	+30/-10	±10	±15		26
	Ripple	012	PS1	_	- 6	+30/-10	±15	±15	mV	3, 6,
		oge,	PS2	_	H	+30/-10	+30/-10	+30/-10	eo.	
		A Ulli	PS3	700	_	+30/-10	+30/-10	+30/-10		
ined I	DC_LL	Loadline slope within the VR regulation loop capability	S-Processor Line	-	I		2.1 Unde	ined une	mΩ	10,1 14
ige,	AC_LL	AC Loadline	S-Processor Line	_	-	Same	up to 400 KHz)	mΩ	10,13 14	
	T_OVS_TD P_Max	Max Overshoot time TDP/virus mode	led m.	_	define	d unde	10/30	4	μs	und
	V_OVS TDP_Max/ virus_Max	Max Overshoot at TDP/virus mode		eg ni	_		70/200	sed mider	mV	

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management
- event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states). The voltage specification requirements are measured across Vcc_SENSE and Vss_SENSE as near as possible to the processor with a 20 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and $1~M\Omega$ minimum impedance. The maximum length of ground 3. wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
- Processor IA core VR to be designed to electrically support this current.
- Processor IA core VR to be designed to thermally support this current indefinitely.
- Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
- Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
- PSx refers to the voltage regulator power state as set by the SVID protocol.
- N/A
- LL measured at sense points.
- Typ column represents ICCmax for commercial application it is NOT a specification it is a characterization of limited samples using limited set of benchmarks that can be exceeded.
- Operating voltage range in steady state.
- LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected. 13.
- undefined undefi By Improving Load Line (Lower LL than EDS values, and reporting it to BIOS), customers may obtain slightly better performance; a), although, the frequencies will not be changed. .ci

ined undefined l



7.2.1.2 **Vcc_{GT} DC Specifications**

Processor Graphics (Vcc_{GT}) Supply DC Voltage and Current Specifications (Sheet 1 of 2) **Table 7-3.**

		(511)	550 1 50 2)							
	Symbol	Parameter	Segment	Min.	Тур.	"uge,	Max.		Unit	Note ¹
	Operating voltage	Active voltage Range for Vcc _{GT}	All	0.55	efired	<i>3</i> .	1.5	2013	ov	2,3,6,8
	Idle voltage	Processor Graphics core idle voltage	All	0	-		0.55	-d under	V	3
	Non		S(35W)-dual core GT _{2/1}				48	lues		
	J*		S(51W)-dual core GT ₂				48			
fined			S(51W) - dual core GT ₁ Pentium [®] /Celeron [®]			60	48			
			S(54W) -dual core GT ₁			"Joe,	48			light.
	I _{CCMax_GT}	Max Current for Processor Graphics Rail	S(54W) - dual core GT ₁ Pentium [®] /Celeron [®]	_	eined	O.	48		A	6
		, nuo	S(25W) - quad core GT ₂		Yej,,		35	Tipe:		
	00	9	S(35W)-quad core GT ₂	7 010			35	'Wale		
	46/11/10		S(65W) - quad core GT _{2/1}				45	eg m.		
	UNO		S(80W)-quad core GT ₂				45	iine		
			S(95W)-quad core GT ₂ K-SKU				45	*		
stined	TO D	Vcc _{GT}	PS0,PS1	_	_		±20		mV	3,4
	TOB _{GT}	Tolerance	PS2,PS3	_	_	10	±20		mV	3,4
		Ripple	-9 on -	1	1	$I_L \leq 0.5$	0.5 <i<sub>L<i<sub>CCTDC</i<sub></i<sub>	I _{CCTDC} <i<sub>L<iccmax< td=""><td></td><td>76/</td></iccmax<></i<sub>		76/
		Tolerance	PS0	_	0	+30/-10	±10	±15	•	nu _c
	Ripple	"ye,	PS1	_	104111	+30/-10	±15	±15	mV	3,4
		901.	PS2	(1	10,-	+30/-10	+30/-10	+30/-10		
	nia		PS3	SQ	_	+30/-10	+30/-10	+30/-10		
	DC_LL	vcc _{GT} Loadline slope	S-Processor Line	_	_		3.1	efines	mΩ	7,9,10
	AC_LL	AC Loadline	S-Processor Line	_	_	Same	as Max DC_LL (up to 400 KHz)	mΩ	7,9,10
	T_OVS_Max	Max Overshoot time	- undefine	-	_	- 69	fine 10		μs	
	V_OVS_Max	Max Overshoot	160	_	-	ed une	70		mV	nugis
		ed under			indefili			ade	ine	,
	d undefil		ined undefined undefi					fined une		
efine			ined und				dung			
			, hugein,				efine			A 4
			ined			ied nu				d und
	Datashe	et, Volume 1 of	2	4	undefil			idefined und	3fine	5
	adel	ist, voiding 1 01	-	ined				ined une	11,	•
	Datashe		ad unde					Igetin,		
16,111			eine							



Processor Graphics (VCCGT) Supply DC Voltage and Current Specifications **Table 7-3.** (Sheet 2 of 2)

Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Note ¹
					20,		

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep® Technology, or low-power states). The voltage specification requirements are measured across Vcc_{GT} _SENSE and Vsc_{GT} _SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M Ω minimum impedance. The maximum length of ground
- wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
- PSx refers to the voltage regulator power state as set by the SVID protocol.
- Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep® Technology, or low-power states).
- N/A
- LL measured at sense points.
- Operating voltage range in steady state.
- LL specification values should not be exceeded. If exceeded, power, performance, and reliability penalty are expected.
- By Improving Load Line (Lower LL than EDS values, and reporting it to BIOS), customers may obtain slightly better performance although the frequencies will not be changed.

V_{DDO} DC Specifications

Table 7-4. Memory Controller (V_{DDO}) Supply DC Voltage and Current Specifications

		1	1	1	10°	1	1 -	1
Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Note ¹	
V _{DDQ (DDR3L/-RS)}	Processor I/O supply voltage for DDR3L/-RS	All	Typ-5%	1.35	Typ+5%	V	3,4,5	ciro
V _{DDQ (DDR4)}	Processor I/O supply voltage for DDR4	All	Typ-5%	1.20	Typ+5%	V	3,4,5	indefill
TOB _{VDDQ}	VDDQ Tolerance	All	10	AC+DC: ± 5	5	%	3,4	3.00
Icc _{MAX_VDDQ} (DDR3L/-RS)	Max Current for V _{DDQ} Rail (DDR3L/-RS)	s unde	_	_	2.8	Α	2	
Icc _{MAX_VDDQ} (DDR4)	Max Current for V _{DDQ} Rail (DDR4)	Seines	_	_	2.8	A	2	

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- The current supplied to the DIMM modules is not included in this specification.
- No requirement on the breakdown of AC versus DC noise.
- undefined undefi The voltage specification requirements are measured with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and $1-M\Omega$ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. allos undefined undefined



7.2.1.4 Vcc_{SA} DC Specifications

Table 7-5. System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Note ^{1,2}
Vcc _{SA}	Voltage for the System Agent	S-Processor Line (fixed voltage)	_	1.05	under -	V	3,5
TOB _{VCCSA}	V _{CCSA} Tolerance	S-Processor Line	-6	efine	±50(DC+AC+ripple)	mV	3
I _{CCMAX_} VC CSA	Max Current for V _{CCSA} Rail	S-Processor Line) The	_	11.1	А	
AC_LL	AC Loadline	S-Processor Line	_	_	Same as Max DC_LL (up to 400 KHz)	mΩ	6,7
T_OVS_ Max	Max Overshoot time	isfined un	_	_	10	μs	
V_OVS_ Max	Max Overshoot	d nuge -	_	_	70	mV	76

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- Long term reliability cannot be assured in conditions above or below Max./Min functional limits.
- The voltage specification requirements are measured on Vcc_{SA} SENSE and Vss_{SA} SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
- PSx refers to the voltage regulator power state as set by the SVID protocol. VCC_{SA} voltage during boot (Vboot)1.05V for a duration of 2 seconds. LL measured at sense points.

- LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.

Vcc_{IO} DC Specifications 7.2.1.5

Processor I/O (Vcc_{IO}) Supply DC Voltage and Current Specifications

.//			407.				
Symbol	Parameter	Segment	Min.	Min. Typ.		Unit	Note ^{1,2}
V _{CCIO}	Voltage for the memory controller and shared cache	s define	_	0.95	_	V	3,4,5,6
TOB _{VCCIO}	V _{CCIO} Tolerance	All		AC+DC: ±50		mV	3
I _{CCMAX_VCCIO}	Max Current for V _{CCIO} Rail	S	_	_	5.5	Α	
T_OVS_Max	Max Overshoot time	All	_	-inde	100	uS	7
V_OVS_Max	Max Overshoot at TDP	All	-	wed or	20	mV	7

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- Long term reliability cannot be assured in conditions above or below Max/Min. functional limits.
- The voltage specification requirements are measured across Vc_{IO} _SENSE and Vs_{IO} _SENSE as near as possible to the processor with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. For low BW bus connection between processor and PCH -> $V_{\rm CCIO}$ =0.85V. For high BW bus connection between processor and PCH -> $V_{\rm CCIO}$ =0.95V.

- OS occurs during power on only. not during normal operation

. A . madefined undefined undefined Datasheet, Volume 1 of 2



7.2.1.6 Vcc_{ST} DC Specifications

Table 7-7. Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

			16					
Symbol	Parameter	Se	gment	Min.	Тур.	Max.	Units	Notes 1,2
Vcc _{ST}	Processor Vcc Sustain supply voltage	All	i a	UGO.	1.0	_	V	3
TOB _{ST}	V _{CCST} Tolerance	All	"Uge	A	AC+DC: ± 5		mV	3
Icc _{MAX_ST}	Max Current for Vcc _{ST}	S	900	_	_	60	mA	4

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These
 specifications will be updated with characterized data from silicon measurements at a later date.
- 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
- 3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and $1-M\Omega$ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

Table 7-8. Vcc Sustain Gated (Vcc_{STG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Тур.	Max.	Units	Notes 1,2
Vcc _{STG}	Processor Vcc Sustain Gated supply voltage	All	_	1.0	_	V	3
TOB _{STG}	V _{CCSTG} Tolerance	All		AC+DC: ±5	ç.	mV	3
Icc _{MAX_STG}	Max Current for Vcc _{STG}	S	_	_	20	mA	4

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These
 specifications will be updated with characterized data from silicon measurements at a later date.
- 2. Long term reliability cannot be assured in conditions above or below Max./Min functional limits.
- 3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and $1\text{-M}\Omega$ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.1.7 Vcc_{PLL} DC Specifications

Table 7-9. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications

	76					-	
Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Notes ^{1,2}
V _{CCPLL}	PLL supply voltage (DC + AC specification)	All	_	1.0	_	V	3
TOB _{CCPLL}	V _{CCPLL} Tolerance	All	A	AC+DC: ±	5	mV	3
I _{CCMAX_VCCPLL}	Max Current for V _{CCPLL} Rail	S	Fined.	_	150	mA	

Notes:

- 1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
- 3. The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M Ω minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.



Table 7-10. Processor PLL OC (Vcc_{PLL OC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Тур.	Max.	Unit	Notes ^{1,2}
V _{CCPLL_OC}	PLL OC supply voltage (DC + AC specification)	All	- 41	VDDQ	_	V	3
TOB _{CCPLL_OC}	V _{CCPLL_OC} Tolerance	All	AC+DC:± 5		5	mV	3
I _{CCMAX_} VCCPLL_OC	Max Current for V _{CCPLL_OC} Rail	S-dual core GT2 S-quad core GT2			100 130	mA	ed ur

Notes:

- Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
- Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
- The voltage specification requirements are measured on package pins with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and $1-M\Omega$ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.

7.2.2 **Processor Interfaces DC Specifications**

7.2.2.1 **DDR3L/-RS DC Specifications**

Table 7-11. DDR3L/-RS Signal Group DC Specifications (Sheet 1 of 2)

	ed		S-	-Processor Li	ne	71	96,
.0	Symbol	Parameter	Min.	Тур.	Max.	Units	Notes ¹
od uli	V _{IL}	Input Low Voltage	_	V _{DDQ} /2	0.43*V _{DDQ}	V	2, 4, 9, 10
Sine	V _{IH}	Input High Voltage	0.57*V _{DDQ}	V _{DDQ} /2	7 170	V	3, 4, 9, 10
undefined un	R _{ON_UP/DN(DQ)}	DDR3L/-RS Data Buffer pull-up/down Resistance		Trainable	160	Ω	12
	R _{ODT(DQ)}	DDR3L/-RS On-die termination equivalent resistance for data signals		Trainable		Ω	12
	V _{ODT(DC)}	DDR3L/-RS On-die termination DC working point (driver set to receive mode)	0.45*V _{DDQ}	0.5*V _{DDQ}	0.55*V _{DDQ}	V	12 00
	R _{ON_UP/DN(CK)}	DDR3L/-RS Clock Buffer pull-up/down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 12
d undefined ur	R _{ON_UP/DN} (CMD)	DDR3L/-RS Command Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	12
adefine	R _{ON_UP/DN(CTL)}	DDR3L/-RS Control Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 12
g ull.	R _{ON_UP/DN} (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	-inder	140	Ω	
	I ^{II}	Input Leakage Current (DQ, CK) 0 V 0.2*V _{DDQ} 0.8*V _{DDQ}	, undefir	- eg -	1	mA	adefined
ed undefined u	Indefili	0.2*V _{DDQ} 0.8*V _{DDQ}		ed unde	ined unde		
	Datachoot Volume	e 1 of 2	ed undefi			à	undefine
lefined.	unde	ined undefi	*		ad und	efineu	unde ^{fine}



Table 7-11. DDR3L/-RS Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	S	-Processor Li	Units	Notes ¹	
Symbol	Farameter	Min.	Тур.	Max.	Onics	Notes
DDR0_Vref_DQ DDR1_Vref_DQ DDR_Vref_CA	VREF output voltage	Trainable	VDDQ/2	Trainable	V	13, 14

Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- $V_{\rm IL}$ is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
- VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- $V_{IH}^{\rm II}$ and V_{IL} may experience excursions above $V_{\rm DDQ}$. However, input signal drivers must comply with the signal quality
- This is the pull-up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
- DDR_DRAMPWROK must have a maximum of 15 ns rise or fall time over $V_{DDQ} * 0.30 \pm 100$ mV and the edge must be monotonic.

- DDR_VREF is defined as V_{DDQ}/2 for DDR3L/-RS R_{ON} tolerance is preliminary and might be subject to change.

 Max-min range is correct but center point is subject to change during MRC boot training. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods. 10.

- Final value determined by BIOS power training, values might vary between bytes and/or units. VREF values determined by BIOS training, values might vary between units. DDR0_Vref_DQ Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0.

7.2.2.2 **DDR4 DC Specifications**

Table 7-12. DDR4 Signal Group DC Specifications (Sheet 1 of 2)

undefined	Combal	Parameter	S	-Processor L	ine	II-it-	Notes ¹	undefined ur
Unc.	Symbol	Parameter	Min.	Тур.	Max.	Units	Notes*	sineo
	V _{IL}	Input Low Voltage	0	VREF(INT)	VREF(INT) - 0.07*VDDQ	V	2, 4, 9, 10, 14	nuge.
	N ^{IH}	Input High Voltage	VREF(INT) + 0.07*VDDQ	VREF(INT)	-	V	3, 4, 9, 10, 14)·
	R _{ON_UP/DN(DQ)}	DDR4 Data Buffer pull-up/ down Resistance		Trainable		Ω	12	
	R _{ODT(DQ)}	DDR4 On-die termination equivalent resistance for data signals		Trainable	i efi	Ω	12	-
isfined	V _{ODT(DC)}	DDR4 On-die termination DC working point (driver set to receive mode)	0.45*V _{DDQ}	0.5*V _{DDQ}	0.55*V _{DDQ}	V	10	
Jundefined L	R _{ON_UP/DN(CK)}	DDR4 Clock Buffer pull-up/ down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 12	undefinedu
	R _{ON_UP/DN(CMD)}	DDR4 Command Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	12	under
	R _{ON_UP/DN(CTL)}	DDR4 Control Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 12	0.
	R _{ON_UP/DN} (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	_	140	Ω	uge.	-
ed undefined	I	Input Leakage Current (DQ, CK) 0 V 0.2*V _{DDQ} 0.8*V _{DDQ}	_	_	ed under	mA	-	
ed unc	120 undefined und	0.8*V _{DDQ}	::ne	d undefil				ed undefined
	120 sined uno		nuge _{II} .		Data		lume 1 of 2	
o de la companya de l	I hugei.	d undefine			,ndf	fined		
18fill		sine o			ad ui.			



Table 7-12. DDR4 Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	S	Units	Notes ¹			
Symbol	Pai ameter	Min.	Тур.	Max.	Offics	Notes	
DDR0_VREF_DQ	VREF output voltage	<u> </u>	elli				
DDR1_VREF_DQ	V OI.	Trainable	VDDQ/2	Trainable	V	13,15	
DDR_VREF_CA		900					

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- V_{1L} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
- V_{1H}^{r} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
- $V_{
 m IH}^{
 m i}$ and $V_{
 m IL}$ may experience excursions above $V_{
 m DDO}$. However, input signal drivers must comply with the signal quality
- This is the pull-up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
- DDR_DRAMPWROK must have a maximum of 15 ns rise or fall time over $V_{DDQ} * 0.30 \pm 100$ mV and the edge must be monotonic.
- 8.
- DDR_VREF is defined as $V_{\rm DDQ}/2$ for DDR4 $R_{\rm ON}$ tolerance is preliminary and might be subject to change. Max-min range is correct but center point is subject to change during MRC boot training. 10.
- Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
- 12.
- Final value determined by BIOS power training, values might vary between bytes and/or units.

 VREF values determined by BIOS training, values might vary between units.

 VREF(INT) is a trainable parameter where the value is determined by BIOS for margin optimization.
- DDR0_Vref_DQ Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0

7.2.2.3 PCI Express* Graphics (PEG) DC Specifications

Table 7-13. PCI Express* Graphics (PEG) Group DC Specifications

Symbol	Parameter	Min.	Тур.	Max.	Units	Notes ¹
Z _{TX-DIFF-DC}	DC Differential Tx Impedance	80	100	120	Ω	1, 5
Z _{RX-DC}	DC Common Mode Rx Impedance	40	50	60	Ω	1, 4
Z _{RX-DIFF-DC}	DC Differential Rx Impedance	80	_	120	Ω	1
PEG_RCOMP	resistance compensation	24.75	25	25.25	Ω	2, 3

Notes:

- Refer to the PCI Express Base Specification for more details.
- Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
- PEG_RCOMP resistance must be provided on the system board with 1% resistors. COMP resistors are to VCCIO. PEG_RCOMP- Intel allows using 24.9 Ω 1% resistors.
- DC impedance limits are needed to ensure Receiver detect.
- Indefined undefined undefi The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.

Jumdefined undefined undef . A . madefined undefined undefined Datasheet, Volume 1 of 2 .ed undefi



Digital Display Interface (DDI) DC Specifications 7.2.2.4

Table 7-14. Digital Display Interface Group DC Specifications (DP*/HDMI*)

	-4/2						
Uc	Symbol	Parameter	Min	Тур.	Max.	Units	Notes ¹
	V _{IL}	Aux Input Low Voltage	- 110,	_	0.8	V	
	V _{IH}	Aux Input High Voltage	2.25	_	3.6	V	-61
	V _{OL}	DDIB_TXC[3:0] Output Low Voltage DDIC_TXC[3:0] Output Low Voltage DDID_TXC[3:0] Output Low Voltage	_	_	0.25*V _{CCIO}	V	1,2
defined ur	V _{OH}	DDIB_TXC[3:0] Output High Voltage DDIC_TXC[3:0] Output High Voltage DDID_TXC[3:0] Output High Voltage	0.75*V _{CCIO}	_	ndefine	V	1,2
18iin	Z _{TX-DIFF-DC}	DC Differential Tx Impedance	100	- 2	120	Ω	
ILUOR	Notes: 1. V _{CCIO} depends	on segment.	_	define			

embedded DisplayPort* (eDP*) DC Specification 7.2.2.5

Table 7-15. embedded DisplayPort* (eDP*) Group DC Specifications

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{OL}	eDP_DISP_UTIL Output Low Voltage	\(\sigma'\)	77	0.1*V _{CCIO}	V
V _{OH}	eDP_DISP_UTIL Output High Voltage	0.9*V _{CCIO}	-	_	V
R _{UP}	eDP_DISP_UTIL Internal pull-up	100	_	_	Ω
R _{DOWN}	eDP_DISP_UTIL Internal pull-down	100	_	_	Ω
eDP_RCOMP	eDP resistance compensation	24.75	25	25.25	Ω
Z _{TX-DIFF-DC}	DC Differential Tx Impedance	80	100	120	Ω

 V_{CCIO} depends on segment. V_{OL} and V_{OH} levels depends on the level chosen by the Platform.

COMP resistance is to VCOMP_OUT.



7.2.2.6 CMOS DC Specifications

Table 7-16. CMOS Signal Group DC Specifications

Symbol	Parameter	Min.	Max.	Units	Notes ¹
V _{IL}	Input Low Voltage	4/10	Vcc * 0.3	V	2
V _{IH}	Input High Voltage	Vcc * 0.7	_	V	2, 4
V _{OL}	Output Low Voltage	-	Vcc * 0.1	V	2
V _{OH}	Output High Voltage	Vcc * 0.9	_	V	2, 4
R _{ON}	Buffer on Resistance	23	73	Ω	-
I _{LI}	Input Leakage Current	_	±150	μΑ	3

Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- The Vcc referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$. 2.
- 3. For VIN between "0" V and Vcc_{ST}. Measured when the driver is tri-stated.
- V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers must comply with the signal quality specifications.

GTL and OD DC Specifications

Table 7-17. GTL Signal Group and Open Drain Signal Group DC Specifications

Symbol	Parameter	Min.	Max.	Units	Notes ¹
V _{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	-	Vcc * 0.6	V	2
V _{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc * 0.72	_	V	2, 4
V _{IL}	Input Low Voltage (PROC_TCK,PROC_TRST#)	2011	Vcc * 0.3	V	2
V _{IH}	Input High Voltage (PROC_TCK,PROC_TRST#)	Vcc * 0.3	_	V	2, 4
V _{HYSTERESIS}	Hysteresis Voltage	Vcc * 0.2	_	V	Sil.
R _{ON}	Buffer on Resistance (TDO)	7	17	Ω	_
V _{IL}	Input Low Voltage (other GTL)	_	Vcc * 0.6	V	2
V _{IH}	Input High Voltage (other GTL)	Vcc * 0.72	- 18/11	V	2, 4
R _{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	-
R _{ON}	Buffer on Resistance (other GTL)	12	28	Ω	-
I _{LI}	Input Leakage Current	- 10	±150	μΑ	3

Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- The Vcc_{ST} referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.
- 3. For VIN between 0 V and Vcc_{ST}. Measured when the driver is tri-stated.
- V_{IH} and V_{OH} may experience excursions above V_{CCST} . However, input signal drivers must comply with the signal quality specifications.

. A . radefined undefined undefined Datasheet, Volume 1 of 2



7.2.2.8 **PECI DC Characteristics**

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 7-18. PECI DC Electrical Limits

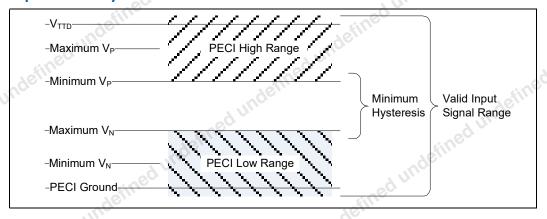
					<u> </u>	
	Symbol	Definition and Conditions	Min.	Max.	Units	Notes ¹
dell	R _{up}	Internal pull-up resistance	15	45	Ω	3
d Ulli	V _{in}	Input Voltage Range	-0.15	Vcc _{ST} + 0.15	V	-
	V _{hysteresis}	Hysteresis	0.15 * Vcc _{ST}	7/10	V	-
ndefined undefined L	V _{IL}	Input Voltage Low- Edge Threshold Voltage	_	0.3 * Vcc _{ST}	V	-
	V _{IH}	Input Voltage High- Edge Threshold Voltage	0.7 * Vcc _{ST}	_	٧	-
	C _{bus}	Bus Capacitance per Node	N/A	10	pF	- 8
	C _{pad}	Pad Capacitance	0.7	1.8	pF	citles
ad vi.	Ileak000	leakage current @ 0V	_	0.6	mA	16,-
	Ileak025	leakage current @ 0.25* Vcc _{ST}	_	0.4	mA	-
	Ileak050	leakage current @ 0.50* Vcc _{ST}	_	0.2	mA	-
ed ull	Ileak075	leakage current @ 0.75* Vcc _{ST}	_	0.13	mA	-
	Ileak100	leakage current @ Vcc _{ST}	_	0.10	mA	-
undefined undefined un	The leakag	lies the PECI interface. PECI behaves specification applies to powered ouffer internal pull-up resistance m	devices on the PEC	CI bus.	pecifications.	

- Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} min/max specifications.
- The leakage specification applies to powered devices on the PECI bus. The PECI buffer internal pull-up resistance measured at 0.75* Vcc_{ST}.

Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 7-1. **Input Device Hysteresis**





8 Package Mechanical Specifications

8.1 Package Mechanical Attributes

The S-Processor Line uses a Flip Chip technology available in Land Grid Array (LGA). The following table provides an overview of the mechanical attributes of the package. For specific dimensions (die size, die location, and so on), refer to the processor package mechanical drawings (see Related Documents section).

Table 8-1. Package Mechanical Attributes

	Package	Parameter	S-Processor Line	
	60	700	Quad Core /Dual Core GT2	~geII.
		Package Type	Flip Chip Land Grid Array	
inde	Package	Interconnect	Land Grid Array (LGA)	
ndefined undefined uno	Technology	Lead Free	N/A	
ie fine		Halogenated Flame Retardant Free	Yes	
IIIOS		Solder Ball Composition	N/A	
		Ball/Pin Count	1151	
18fills	De also do	Grid Array Pattern	Grid Array	110
	Package Configuration	Land Side Capacitors	Yes	ed.
	4 Uli	Die Side Capacitors	No	refil.
A	efines	Die Configuration	1 Die Single-Chip Package with IHS	nuc.
, nue	Package	Nominal Package Size	37.5x37.5 mm	
ineo -	Dimensions	Min Ball/Pin pitch	0.914 mm	
Jundefined undefined un	od ur	defined undefine	undefined undefined &	adefined U



led undefined undefined **Package Storage Specifications** 8.2

Table 8-2. Package Storage Specifications

intel		, undefined Pa	ickage Mecl	hanical Spec	ifications	
taed und 8.2	Package St	orage Specifications	indefin	ed m.		
Table 8-2.	Package Storage		N.	Mari	None	l sed u
	Parameter	Description	Min.	Max.	Notes	i e fill
, in ⁱ	T _{ABSOLUTE} STORAGE	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time.	-25 °C	125 °C	1, 2, 3	Inde
	T _{SUSTAINED} STORAGE	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5	
, under	RH _{SUSTAINED} STORAGE	The maximum device storage relative humidity for a sustained period of time.	60% (@ 24 °C	5, 6	
	TIME _{SUSTAINED} STORAGE	A prolonged or extended period of time: typically associated with customer shelf life.	0 months	6 months	6	
	connected to a vol	nent device that is not assembled in a board or soci			•	lefined!

Notes:

- Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
- Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC standards.
- TABSOLUTE STORAGE applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
- Intel-branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
- The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
- 126 Indefined under the dunder th able Interpretation of the control o Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{\text{SUSTAINED STORAGE}}$ and customer shelf life in applicable Intel boxes and bags.



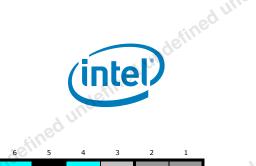
Processor Land Information

Ine processor is available in the LGA package (LGA1151). Figure 9-1, Figure 9-2, Figure 9-3, and Figure 9-4 provide a top view of the Land map per quadrant. Table 9-1 provides the Land list. .. Table 9-.. Table 9-

hume 1 of 2 Datasheet, Volume 1 of 2 istined undefi



ger.					on.	elin							1e ^f	Weg							eine
	/	nt	el,	ned	O.							ed u	ndefi		F	Process	sor La	nd Inf	ormat		efine
										und	leţii.							inde ^f	inec		
nu .	Figu	ıre 9	-1.	Land	Мар	(Тор	Viev	w, Up	per-) Left (Quad	rant))			nij _o	eq.				
ndefined un	40	39	38	37	36	35	34	33	32	31 DDR0 E	30	29 DDR1_C	28 DDR1_M A[14] / DDR1 C	27	26 DDR1_M A[7] / DDR1_C	DDR1 A	24 DDR0_C	23 VDDQ	22	21	20
A				DDR0 D		DDR0 D				CC[7]		KE[0]	A[14] / DDR1 C AA[9] / DDR1 B G[1] DDR1 B A[2] /	DDR1_M A[9] /	AA[4] / DDR1_M A[7]	LERT#	KE[0]	DDRO B			1 etir
AW			RSVD_T	Q[24] / DDR0_D Q[40]		Q[27]/ DDR0_D Q[43]		DDR0_E CC[2]		DDR0_E CC[6]		DDR1_C KE[2]	A[2] / DDR1_C AA[5]/ DDR1_B G[0]	A[9]/ DDR1_C AA[1]/ DDR1_M A[9]	A[6] / DDR1_C AA[2] / DDR1_M A[6]	VDDQ		AA[5]/ DDR0_B G[0]	DDR0 M	y un	DDR0_M
AV	130	RSVD_T		DDR0_D Q[29] / DDR0_D Q[45]	DDR0_D QSP[3] DDR0_D QSP[5]	DDR0_D Q[26] / DDR0_D Q[42]		DDR0_E CC[5]	DDR0_D QSP[8]	DDR0_E CC[3]		DDR1_C KE[1]		A[12] / DDR1_C AA[6] / DDR1_M A[12]		DDR0_C KE[3]	DDR0_C KE[2]	A[14] / DDR0_C AA[9]/ DDR0_B G[1]	DDR0_M A[12] / DDR0_C AA[6] / DDR0_M A[12]	\/DD0	A[6] / DDR0_C AA[2] / DDR0_M A[6]
AU	RSVD	RSVD	DDR0_D Q[25] / DDR0_D Q[41]	DDR0_D Q[28] / DDR0_D Q[44]	DDR0_D QSN[3] DDR0_D QSN[5]	DDR0_D Q[31] / DDR0_D Q[47]		DDR0_E CC[0]	DDR0_D QSN[8]	DDR0_E CC[4]		DDR1_C KE[3]	DDR1_M A[15] / DDR1_C AA[8]/ DDR1_A CT#		DDR1_M A[8] / DDR1_C AA[3] / DDR1_M		DDR0_M A[15] / DDR0_C AA[8]/ DDR0_A CT#	VDDQ	DDR0_M A[11] / DDR0_C AA[7] / DDR0_M A[11]	DDR0_M A[7] / DDR0_C AA[4] / DDR0_M	DDR0_M A[5] / DDR0_C AA[0] / DDR0_M
AT	П					DDR0_D Q[30] / DDR0_D Q[46]		DDR0_E CC[1]					CI#	A[II]	A[O]		CI#	DDR0_A LERT#	DDR0_M A[9] / DDR0_C AA[1] / DDR0_M	VDDO	DDR0_M A[8] / DDR0_C AA[3] / DDR0_M
AR	DDR0_D Q[23] / DDR0_D	Q[22]/	Q[18] / DDR0 D	DDR0_D Q[19] / DDR0_D		Q[46]						DDR1_D Q[27]/ DDR0_D	Q[30] / DDR0_D		DDR1_E CC[1]	DDR1_E CC[0]		VSS	A[9]		A[8]
АР	Q[39]	Q[38] DDR0_D QSN[2] DDR0_D	Q[34] DDR0_D QSP[2] DDR0_D	Q[35]		DDR1_D Q[16] / DDR0_D Q[48]	DDR1_D Q[21] / DDR0_D Q[53]	DDR1_D QSP[2] / DDR0_D QSP[6]	DDR1_D Q[19] / DDR0_D Q[51]	DDR1_D Q[23] / DDR0_D Q[55]		Q[59] DDR1_D Q[26] / DDR0_D Q[58]	Q[62] DDR1_D Q[31] / DDR0_D Q[63]		DDR1_E CC[4]	DDR1_E CC[5]		DDR1_M A[4]	DDR1_C KP[1]	DDR1_C KN[1]	DDR1_C KN[3]
AN	DDR0_D	QSN[4] DDR0_D Q[20] / DDR0_D Q[36]	QSP[4] DDR0_D Q[16] / DDR0_D Q[32]	DDR0_D Q[21] / DDR0_D Q[37]		DDR1 D	DDR1 D	DDR1_D	DDR1_D Q[18]/	-0		DDR1_D QSN[3]	DDR1_D QSP[3] / DDR0_D QSP[7]		DDR1_D QSN[8]	DDR1_D QSP[8]				DDR1_C KN[2]	DDR1_C KP[2]
undefined an								S2M[0]					DDR1_D Q[28] / DDR0_D Q[60]		DDR1_E CC[2]	DDR1_E CC[3]		DDR1_M A[3]	DDR1_M A[2] / DDR1_C AB[5]/ DDR1_M	DDR1_C KN[0]	DDR1_C KP[0]
Uno	DDR0_D	DDR0_D	DDR0_D Q[10]	DDR0_D		DDR1_D Q[9] / DDR0_D	DDR1_D Q[13]/ DDR0_D	DDR1_D QSP[1]	DDR1_D Q[11] /	DDR1_D Q[15] / DDR0_D Q[31]		DDR1 D	DDR1_D Q[29] / DDR0_D		DDR1_E	DDR1_E CC[6]		DDR1 M	DDR1_M A[2] DDR1_M A[1] / DDR1_C AB[8]/ DDR1_M		DDR1_P
AK			DDR0_D QSP[1]	113		Q[25] DDR1_D Q[8] / DDR0_D	DDR1 D	DDR1_D	DDR1 D	DDR1 D		Q[56]	Q[61]	RSVD	CC[/]	cc[o]		DDR1_M A[5]	DDR1_M A[1]	RSVD	AN
AA LA		0	QSP[1] DDR0_D Q[8]			DĎŘŐ_D Q[24]	DĎR0 <u>^</u> D Q[28]	DDR0_D QSN[3]	DĎR0 <u>1</u> D Q[26]	DĎR0 <u>^</u> D Q[30]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		VCC	VCC	VCC
АН						Q[3] / DDR0_D Q[19]	DDR1_D Q[7] / DDR0_D Q[23] DDR1_D		9e,,							69	fine				
AH AG AF	DDR0_D Q[7]		DDR0_D Q[2]	DDR0_D Q[3]		Q[2] / DDR0_D Q[18]	Q[6] / DDR0_D Q[22] DDR1_D QSN[0]							ilo.	red'	77.					
		QSN[0]		DDR0 D		DDR0_D QSP[2]	DDR0_D QSN[2]					-0	ال نار	ge.							nug _s
AE AD	Q[5]	Q[4]	DDR0_D Q[0]	Q[1]		Q[4] / DDR0_D Q[20] DDR1_D Q[1] / DDR0_D Q[17]	Q[21]		Н		und	Still.							,de ⁽ⁱ	neo	
AC		DDR1_V REF_DQ		RSVD	DDR_VT T_CNTL				ae ^s i	Med							****	30. N			
AB AA			VCCGT	VCCGT	ELECT#	#	VCCGT	VCCGT								und	6,,				
ad undefin a						und	eil.							ndei	ine						۸
				nde	inec							, efil	ed u								Jund
ed undefina	128	Vije.	led !), .							y nu		edu			Da			ıme 1 d	of 2	
6	nu b							4	unde							d un		Jen.			
1efin							chi	UEQ.								g an					

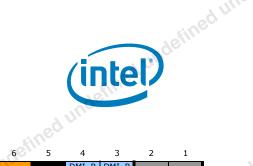


ger.		sined undefine										efin	SQ						::ne
	Process	sor Laı	nd Info	ormatic	on					t Qua	d un					/i F	y to		Jefine
	fined	nu _Q	<i>o-</i>						unde	sfill.							ILE		
ndefined unde	Figure	e 9-2	. La	nd Ma	ар (То	op Vi	ew, U	pper-	-Righ	t Qua	dran	t)			ined				
eined b	19	18	17	16	15	14 DDR0_M A[10] /	13 DDR0_B A[0] /	12	DDR0_C AS#/	10	9	8 DDR0 D	7	6 DDR0 D	5	4 DDR0 D	3	2	1
nde la Ay		VDDQ	DDR0_C KN[1]	VDDQ	DDR0_P AR	DDR0_C AB[7]/ DDR0_M A[10]	DDRO_C AB[4]/ DDRO_B A[0]	VDDQ	DDR0_C AB[1]/ DDR0_M A[15]	DDR0_O DT[3]		Q[32] / DDR1_D Q[0]		Q[39]/ DDR1_D Q[7]		Q[40]/ DDR1_D Q[8]	VSS		-
AW		DDR0_C KP[0]	DDR0_C KP[1]	DDR0_C KP[2]	DDR0_M A[0]/ DDR0_C AB[9]/ DDR0_M A[0] DDR0_B	VDDQ	DDR0_R AS# / DDR0_C AB[3]/ DDR0_M A[16]		DDR0_O DT[0]	VDDQ		DDR0_D Q[33] / DDR1_D Q[1]	DDR0_D QSN[4]/ DDR1_D QSN[0]	DDR0_D Q[38] / DDR1_D Q[6]		DDR0_D Q[45] / DDR1_D Q[13]		RSVD_TP	ger,
AV	A[3]	DDR0_C KN[0]	VDDQ DDR0_M	DDR0_C KN[2]	A[1]7	DDR0_W E#/ DDR0_C AB[2]/ DDR0_M A[14]	DDR0_C S#[2]	DDR0_M A[13] / DDR0_C AB[0] / DDR0_M A[13]	VDDQ	DDR0_C S#[3]		DDR0_D Q[37] / DDR1_D Q[5]	DDR0_D QSP[4] / DDR1_D QSP[0]	DDR0_D Q[34] / DDR1_D Q[2]		DDR0_D Q[41] / DDR1_D Q[9]	DDR0_D Q[44] / DDR1_D Q[12]		RSVD_TP
AU AT	VDDQ	A[1] / DDR0_C AB[8]/ DDR0_M A[1]	A[2]/ DDR0_C AB[5]/ DDR0_M A[2]	DDR0_C KN[3]	VDDQ	DDR0_O DT[1]	VDDQ	DDR0_O DT[2]	DDR0_C S#[1]	RSVD	RSVD	DDR0_D Q[36] / DDR1_D Q[4]		DDR0_D Q[35]/ DDR1_D Q[3]		DDR0_D	DDR0_D QSN[5]/ DDR1_D QSN[1]	QSP[5]/ DDR1_D QSP[1]	DDR0 D
inde ^{ill} at	DDR0_M A[4]	VDDQ		DDR0_C KP[3]	VSS								D			Q[46] / DDR1_D Q[14]	DDR0_D Q[47] / DDR1_D Q[15]	Q[43] / DDR1_D Q[11]	Q[42] / DDR1_D Q[10]
AR					DDR1_M A[13] / DDR1_C AB[0] / DDR1_M A[13]		DDR1_D Q[36] / DDR1_D Q[20]	DDR1_D Q[32] / DDR1_D Q[16]		DDR1_D Q[41] / DDR1_D Q[25]	DDR1_D Q[44] / DDR1_D Q[28]	DDR1_D QSN[5]/ DDR1_D QSN[3]	DDR1_D Q[42] / DDR1_D Q[26]	DDR1_D Q[46] / DDR1_D Q[30]					
АР	DDR1_C KP[3]	DDR1_M A[10] / DDR1_C AB[7]/ DDR1_M A[10]	DDR1_C S#[0]	DDR1_C AS#/ DDR1_C AB[1]/ DDR1_M A[15]	DDR1_O DT[2]		DDR1_D Q[37] / DDR1_D Q[21]	DDR1_D Q[33] / DDR1_D Q[17]		DDR1_D Q[40] / DDR1_D Q[24]	DDR1_D Q[45] / DDR1_D Q[29]	DDR1_D QSP[5]/ DDR1_D QSP[3]	DDR1_D Q[43] / DDR1_D Q[27]	DDR1_D Q[47]/ DDR1_D Q[31]		DDR0_D Q[52] / DDR1_D Q[36]	DDR0_D Q[50] / DDR1_D Q[34]	DDR0_D Q[48] / DDR1_D Q[32]	DDR0_D Q[54]/ DDR1_D Q[38]
AN	Ċ	DDR1_R AS# / DDR1_C AB[3]/ DDR1_M A[16]	DDR1_C S#[2]		DDR1_C S#[1]		DDR1_D QSN[4]/ DDR1_D QSN[2]	DDR1_D QSP[4]/ DDR1_D QSP[2]									DDR0_D QSN[6]/ DDR1_D QSN[4]	DDR0_D QSP[6] / DDR1_D QSP[4]	
undefined un	DDD1 M	DDR1_B A[1]/ DDR1_C AB[6]/ DDR1_B A[1]	DDR1 W	DDR1_O DT[0]	DDR1_C S#[3]		DDR1_D Q[34] / DDR1_D Q[18]	DDR1_D Q[38] / DDR1_D Q[22]		DDR1_D Q[48]	DDR1_D Q[52]	DDR1_D QSN[6]	DDR1_D Q[50]	DDR1_D Q[54]		DDR0_D Q[49] / DDR1_D Q[33]	DDR0_D Q[51] / DDR1_D Q[35]	DDR0_D Q[53] / DDR1_D Q[37]	DDR0_D Q[55] / DDR1_D Q[39]
AL	A[0]/ DDR1_C AB[9]/ DDR1_M A[0]	A[0] / DDR1_C AB[4]/ DDR1_B A[0]	E#/ DDR1_C AB[2]/ DDR1_M A[14]	DDR1_O DT[1]	DDR1_O DT[3]		DDR1_D Q[35] / DDR1_D Q[19]	DDR1_D Q[39] / DDR1_D Q[23]		DDR1_D Q[49]	DDR1_D Q[53]	DDR1_D QSP[6]	DDR1_D Q[51]	DDR1_D Q[55]		DDR0 D	DDR0 D	DDB0 D	DDR0 D
AK						VCCIO			VCCIO							DDR0_D Q[58] / DDR1_D Q[42]	DDR0_D Q[56] / DDR1_D Q[40]	DDR0_D Q[61] / DDR1_D Q[45]	Q[63] / DDR1_D Q[47]
AJ	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCCPLL_ OC		DDR1_D Q[57]	DDR1_D Q[56]			DDR0_D QSN[7]/ DDR1_D QSN[5]	DDR0_D QSP[7] / DDR1_D QSP[5]	
AH AG AF AE						.0	d un	0.					DDR1_D Q[60]	DDR1_D Q[61]		DDR0_D Q[60] / DDR1_D Q[44]	DDR0_D Q[62] / DDR1_D Q[46]	DDR0_D Q[59] / DDR1_D Q[43]	DDR0_D Q[57] / DDR1_D Q[41]
AG AF		-			.00	Silvie							DDR1_D QSP[7] DDR1_D Q[59]	DDR1_D QSN[7] DDR1_D Q[63]			DMI_TXN [3]	DMI_TXP	
				ned	O.						ò		DDR1_D Q[62]	DDR1_D Q[58]	VCCSA		DMI TYP		DMI_TXN [2]
AD AC		. 1	Mye							296	ino	VCCSA	VCCSA		VCCSA_ SENSE DMI_RX N[3]	DMI_RXP [3]	DMI_TXP		DMI_TXN [0]
AB AA	defi	ver.						173.	veg ,	3		VCCSA	VCCSA VCCSA	VCCSA VCCSA	DMI_RX N[1]	DMI_RXP [2] DMI_RXP [1]	DMI_RX N[2]		
aned l'							d u	ige.							idefil				
andefined l				of 2	, un	efin				undf			efin						. 4
			~d\	efine								9 min						· · · · · ·	d und
	Datashe	et, Vol	ume 1	of 2						nug	<i>.</i>						unde	129	
iefined.							4	ndef	In							IUGO			
lefine u						633	led i	<i>P</i> '						~d 1	IU.				

Datasheet, Volume 1 of 2 Jesined undefi



gem	(ii				,nd	efin	0				defil		76	fine	Ò						ć	ined i	71110
	/	1	8	ueg								ed '	11JO			Proc	essor	Land .	Inform				
										. un	defil							6	Lintorn				
		<i>o</i> re 9∹							wer-	-Left	Qua	dran	t)			eš.		Ulli					
ndefined ur	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	1	
uqeili.	w W		VCCGT VCCGT	VCCGT	VCCGT VCCGT		VCCGT VCCGT	VCCGT						0113	90							ined	nue
	v vccgt		VCCGT		VCCGT	J*	VCCGT	VCCGT					ind	9,							.96	illo	
	U VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT	VCCGT VCCGT	VCCGT			- 50	ned								601			
F		VCCGT	200	VCCGT		VCCGT					100,								detit			-	
	P VCCGT	VCCCT	VCCGT	VICCOT	VCCGT	VCCCT	VCCGT	VCCGT	2113	0							-0	July					
	N VCCGT M VCCGT	VCCGT	VCCGT	VCCG1	VCCGT			VCCGT	RSVD		VCC		VCC		VCC	1	VCC		VCC		VCC		
indefined h	L VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	RSVD		RSVD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		und
ing	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT		RSVD	RSVD	RSVD	VCC VCC	VCC	VCC VCC	VCC	VCC	VCC	VCC VCC	VCC	VCC	VCC	VCC VCC	VCC	sine d	
	H VCCGT		VCCGT	Vecer	VCCGT	NOVE	RSVD	RSVD	VCC	VCC	700	VCC	100	VCC	100	VCC	766	VCC	VCC	VCC	CFG[7	3,,	
C	G VCCGT	VCCGT				RSVD	RSVD		VCC		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		CFG[6	CFG[1 2]		
F	F	VCCGT _SENS E	VSSGT _SENS E	RSVD	VSSGT x_SEN SE	RSVD	VCC	VCC	VCC	VCC		VCC		VCC		VCC	VCC	VCC		CFG[1 4]	CFG[1 3]		
E	E VIDSO UT	VIDAL ERT#	VIDSC K		VCC		VCC		VCC		VCC	VCC	VCC	VCC	VCC	VCC	VCC		DDI1_ TXN[1		DDI2 TXN[3		
"ined	D		VSS_S ENSE		VCC	VCC	VCC	VCC	VCC	VCC		VCC		VCC		VCC		DDI1_ TXN[3	DDI1_ TXP[1]	DDI1 TXN[0	DDI2_ TXP[3]		
ndeill	C RSVD	PROC HOT#	VCC_S ENSE		VCC		VCC		VCC		VCC	VCC	VCC	VCC	VCC	VCC		DDI1_ TXP[3]	İ	DDI1_ TXP[0]		0	d un
E	В	RSVD		VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC		VCC		VCC		DDI1_ TXP[2]				efine	
A	A			efil							VCC	VCC	VCC	VCC	VCC	VCC		DDI1_ TXN[2]			I UN		
d undefined		ò	nu,	J							oni.	8//							76	iline		_	
		ines																601					
-6	Inu								1961														
defines) nu							. (1)
Juno						ind	SI							76	ille								
													601									ige,	
				96,								efil											
) nu								undi	3,			
	indi	SI.								ino													
eine								0 V								iu.							
indeli							elin								eine								601
3d 6) UU								indi								defil	
				ye.	ille																601		
Jundefined Jundefine	130		0 v	lu.							15	ge,					Datas	heet \	/olume	1 of 2		idefin indefin	
	255	efin															_ 2003		Jille	5, 2			
	ed nu								undi	S,								ille					
48fin	0						الذع	ueg.								~d U	U						



lqe,,				d uni	defin						d uni	efin	Sq						Fine
	Proces	ssor La	nd Info	ormatio	on						y nu					/ir	nte		
	efined	NUC							unde	3/11									
6-	Figur	e 9-4	. La	nd Ma	ap (T	op Vi	ew. L	ower	-Riah	t Oua	dran	t)			ed	nı.			
ndefined und	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
refile Y					***	SO.						VCCSA	VCCSA	VCCSA		DMI_R XN[0]	DMI_R XP[0]	PCI BC	PCI RC
					9e,								VCCSA		BCLKP	BCLKN	PROC_	LKN PROC	LKP
V				39.0							dur		VCCSA	VCCST	VCCST	VccPLL	AUDIŌ _CLK	AUDIO _SDI	PPOC
U		50.	ein							Sine			VCCSA		PEG_R XP[15]	PEG_R XN[15]		VCCST _PWRG D	PROC_ AUDIO _SDO
Т		9 01							nuc				VCCSA	PEG_R XP[14]	PEG_R XN[14]		PEG_TX N[15]	PEG_TX P[15]	
R								ine'	>				VCCSA	DEC D	PEG_R XP[13]	PEG_R XN[13]	DEC TV	PEG_TX P[14]	PEG_TX N[14]
indefined in P							nde						VCCSA	PEG_R XP[12]	PEG_R XN[12] PEG_R	PEG R	N[13]	PEG_TX P[13] PEG_TX	PEG TX
Aefines N		VCC		VCC		VCC	VCC		CFG_R COMP		eDP_R COMP		VCCSA	PEG_R	XP[11] PEG R	XN[11]	PEG_TX	N[12] PEG TX	P[12]
nuor r	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSVD	COMP	RSVD	COMP	RSVD_	PEG_R COMP	XP[10]	XN[10]	PEG_R XN[9]	N[11]	P[11] PEG_TX	
К		VCC		VCC			RSVD	RSVD	RSVD	RSVD	CLK24P	RSVD_ TP	COMP	PEG_R XP[8]	XP[9] PEG_R XN[8]	XIV[9]	PEG_TX N[9]	N[10] PEG_TX P[9]	P[10]
J	RSVD		RSVD		RSVD	RSVD	RSVD		RSVD		CLK24 N	RSVD_ TP	RSVD_ TP	2.3	PEG_R XP[7]	PEG_R XN[7]	[-]	PEG_TX N[8]	PEG_TX P[8]
н	CFG[15	CFG[5]	CFG[11	CFG[3]	CFG[0]	BPM#[3]	PROC_ TDO	RSVD_ TP	RSVD_ TP	EDP_TX N[2]		VSS		PEG_R XP[6]	PEG_R XN[6]		PEG_TX N[7]	PEG_TX P[7]	
G	3	CFG[18		CFG[8]		BPM#[2]		PROC_ TDI		EDP_TX P[2]	EDP_TX N[3]	VSS	PECI		PEG_R XP[5]	PEG_R XN[5]		PEG_TX N[6]	PEG_TX P[6]
الله الم		CFG[19] DDI2_T	CFG[10	CFG[2]	CFG[1]	CFG[17] CFG[16	PROC_ TMS	PROC_ TRST#	PROC_ TCK	EDP_TX	EDP_TX P[3]	PROCP WRGD PM_SY	RESET	PEG_R XP[4]	PEG_R XN[4] PEG_R	PEG_R	PEG_TX N[5]	PEG_TX P[5] PEG_TX	DEC TV
sineo e		XN[1] DDI2 T	BPM#[CFG[9]		EDP DI	CATER	UXN	THERM	P[0]	EDP TX	NC	#	DEC D	XP[3]	XN[3]	PEG TX	N[4]	P[4] PROC
illige, D	XN[2]	XP[1]	1]	BPM#[0]	RSVD	SP_ŪTI L	R#	EDP_A UXP	TRIP#	N[0]	P[1]	WN		PEG_R XP[2]	PEG_R XN[2]		N[3]		TRIGIN
C	DDI2_T XP[2]		DDI3_T XP[3]		DDI3_T XP[1]		DDI1_A UXN		DDI3_A UXN		EDP_TX N[1]	12	PEG_R XP[1]	PEG_R XN[1]		N[2]	PEG_TX P[2] PROC_		de
В		DDI2_T XP[0]	DDI3_T XN[3]	DDI3_T XP[2]	DDI3_T XN[1]	DDI3_T XP[0]	DDI1_A UXP	DDI2_A UXN	DDI3_A UXP	PROC_ PRDY#	PROC_ PREQ#	PEG_R XP[0]	PEG_R XN[0]		PEG_TX N[1]	PEG_TX P[1]	TDICO	-61	The same
А		DDI2_T XN[0]		DDI3_T XN[2]		DDI3_T XN[0]		DDI2_A UXP		9e,				PEG_TX N[0]	PEG_TX P[0]		170	Ver	
		IEO,							eg n							4 U			
								96fil							717				
sined.							9 ni							חנט .					
indelli					۸	efine													
3.0.					nuc							indi	SI						76
				inec							ined	O.						- 2	
			nuge							79e									
									601	711.									
	iuge,								0										
ined.							-d U												
ndefill						nile.							.:.0						
od m.					un								eill						2
a undefined used undefined												q ou.							nug
			,und							-96	Silling							FINEC	
	Datash	eet, Vol	ume 1	of 2						ULL						ed u	undi	ined	
	inde	11.							IURS							ined			

Datasheet, Volume 1 of 2 ie Undefi



able 9-1. Proc	cessor Land	List (Sheet		d undefined	Processor I	Land Inform	mation
able 9-1. Proc		List (Sheet			60	undefin	
able 9-1. Proc		List (Sheet			6	Ullia	
	essor Land	List (Sheet	1 of 33)				
Land Name			1	T	sine	П	П
	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um
RSVD	"Ugie.			48/11		-16002	2286
VSSGTx_SENSE	900			und		-14173.2	-13258
VSSGT_SENSE			4:0	So		-16002	-13258
VSS_SENSE			deili			-16002	-15087
VSS_SAIO_SENSE			A Ullis			15087.6	4114.
VSS_NCTF		27/2	So			15087.6	-17830
VSS_NCTF		"ger			iefino	-16002	-16916
VSS_NCTF		-9 ni.			INOS	16916.4	-1600
VSS_NCTF	7113	0		_6	d	-17830.8	-15087
RSVD	"uger			16/1/4		-1371.6	8686.
VSS	od u			11100		8686.8	-17830
VSS				CO		6858	-17830
VSS	_		4efil			5029.2	-17830
VSS			, una			3200.4	-17830
VSS	_		Vec.			-3200.4	-17830
VSS		dei			ein's	12344.4	-17830
VSS		4 Une			"Uge,	16002	457.2
VSS	ek'	Vec			ed m	-11430	457.2
VSS	"ge,			717		11430	457.2
VSS	9011			inde		-16916.4	1371.
VSS	ne o			60,0		14173.2	1371.
VSS			10			16002	2286
VSS			11/100			-11430	2286
VSS			· veg			-12344.4	2286
		76			27/2		2286
1		, uno			:/dell.		2286
1		.0e0			-9.711.		3200
	- Ye,				Ve.		3200.
	4000			"Uge,			3200.
1	ILCO.			SQ n.			3200.
10				in			3200.
			, inde				3200.
			reg v.			-40	3200.
AO.	_	26			6.4.1	O.V.	3200.
		' '// _' O',			ade ⁱⁱ		3200.
VSS					4011	12344.4	3200.
	1	(1)		9	Ine.	11430	3200.
VSS		•					
	VSSGT_SENSE VSS_SENSE VSS_SAIO_SENSE VSS_NCTF VSS_NCTF VSS_NCTF RSVD VSS VSS VSS VSS VSS VSS VS	VSSGT_SENSE VSS_SAIO_SENSE VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF RSVD VSS VSS	VSSGT_SENSE VSS_SAIO_SENSE VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF RSVD VSS VSS	VSSGT_SENSE VSS_SENSE VSS_SAIO_SENSE VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF VSS VSS VSS	VSSGT_SENSE VSS_SENSE VSS_SAIO_SENSE VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF VSS_NCTF VSS VSS_NCTF RSVD VSS VSS VSS	VSSGT_SENSE VSS_SENSE VSS_SENSE VSS_SENSE VSS_SENSE VSS_NCTF VS	VSSGT_SENSE -16002 VSS_SENSE -16002 VSS_SAIO_SENSE 15087.6 VSS_NCTF 15087.6 VSS_NCTF -16002 VSS_NCTF -16916.4 VSS_NCTF -17830.8 RSVD -1371.6 VSS -8886.8 VSS -6858 VSS -529.2 VSS -3200.4 VSS -3200.4 VSS -3200.4 VSS -3200.4 VSS -11430 VSS -12244.4 VSS -11430 VSS -11430 VSS -11430 VSS -11430 VSS -11430 VSS -11430



Table 9-1.

gen			indefine			defined			,	ined un
	Pro	ocessor Land Inform	ation			unc		inte	o de	
		, uno			ageil.					
					In.			ING		
	Ta	ble 9-1. Proc	essor Land	List (Sheet	2 of 33)		ined '			
29 U				Inde	1	T	Non-			7
istine	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	interleaved (NIL)	X[um]	Y[um]	,nd
Uge	AE33	VSS	- deill.			rinec	(1112)	-11430	4114.8	ed or
	AE36	VSS	AUC.			"Uge,		-14173.2	4114.8	
	AE5	VSS			0	0		14173.2	4114.8	1
	AE8	VSS			10/1/10	/		11430	4114.8	1
-	AF1	VSS			inde			17830.8	5029.2	1
-	AF33	VSS		-6			2	-11430	5029.2	1
}	AF36	VSS		76/1/1			eine ^O	-14173.2	5029.2	1
601	AF37	VSS		11/10			geili.	-15087.6	5029.2	1
Sine	AF40	VSS		8			un	-17830.8	5029.2	100
inge.	AF40 AF5	VSS	Ae(ill')			Sine!		14173.2	5029.2	ed n.
O. *	AF8	VSS	C ALON			'yell'		11430	5029.2	Sino
		VSS	0)		+	dul.			100	2
	AG1	16/1			017	3		17830.8	5943.6	1
	AG2	VSS			"uge,			16916.4	5943.6	1
	AG3	VSS			d U			16002	5943.6	4
	AG33	VSS		713			· · · · · ·	-11430	5943.6	1
6-	AG36	VSS		11000			defill.	-14173.2	5943.6	<u> </u>
FINE	AG4	VSS		90			a nuc.	15087.6	5943.6	
"uge,	AG5	VSS	76/1/			2013	O.	14173.2	5943.6	9 n
O.	AG8	VSS	1000			4611.		11430	5943.6	dille
	AH33	VSS	20		_	- 01111		-11430	6858	de.
	AH36	VSS			-41	8		-14173.2	6858	<u> </u>
	AH37	VSS			96/.			-15087.6	6858	<u> </u>
	AH38	VSS			od un			-16002	6858	
	AH39	VSS						-16916.4	6858	
à	AH40	VSS		Mye.	_		Aefill.	-17830.8	6858	
sine!	AH5	VSS		69 n.			und	14173.2	6858	
Jundefines	AH8	VSS	113			***	60	11430	6858	ined v
9 011.	AJ1	VSS	"uge.			defill		17830.8	7772.4	tives
	AJ31	VSS	ed -			uns		-9601.2	7772.4	ge.
	AJ32	VSS	>		4	neo.		-10515.6	7772.4	1
	AJ33	VSS			"gel			-11430	7772.4	1
	AJ34	VSS			og un.			-12344.4	7772.4	1
	AJ35	VSS			Nez			-13258.8	7772.4	1
	AJ36	VSS		"uge,			46/11/	-14173.2	7772.4	1
5178	AJ4	VSS		-69 n.			no	15087.6	7772.4	1
ed undefine	AJ5	VSS		Un		44.4	ea	14173.2	7772.4	-81
9 111.	AJ8	VSS	inge.			4641		11430	7772.4	Silver
	AK10	VSS	eq n.			7 nug		9601.2	8686.8	ye.
		101			ined unde				60	7.
		INO			96				Silver	
		tasheet, Volume 1 of 2	2		4 uns			ned und	133	
	ed un	Aefii.						eg n.		
	1 010)\"		ilia.	U		
				eg ni.			inde			
16/11.				ine			9,			



led undefined undefined Processor Land List (Sheet 3 of 33) Table 9-1.

Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
AK12	VSS	"Joejj			18 fine		7772.4	8686.8
AK13	VSS	900			inos		6858	8686.8
AK15	VSS			.:.0	30		5029.2	8686.8
AK16	VSS			deill			4114.8	8686.8
AK17	VSS			A Ulli			3200.4	8686.8
AK18	VSS		213	80		S	2286	8686.8
AK19	VSS		ye,			iefine	1371.6	8686.8
AK20	VSS		od u.			Moo	457.2	8686.8
AK23	VSS	717				,O	-2286	8686.8
AK25	VSS	inde			46411.		-4114.8	8686.8
AK26	VSS	69 0			unc		-5029.2	8686.8
AK28	VSS			2.13	iec,		-6858	8686.8
AK29	VSS			gel.			-7772.4	8686.8
AK30	VSS			od uli.			-8686.8	8686.8
AK36	VSS			Ve.			-14173.2	8686.8
AK37	VSS		age.			de fill	-15087.6	8686.8
AK40	VSS		-69 n.			nuc	-17830.8	8686.8
AK5	VSS	lite				eo	14173.2	8686.8
AK6	VSS	1000			deili		13258.8	8686.8
AK7	VSS	ed			Julia		12344.4	8686.8
AK8	VSS			40	ver.		11430	8686.8
AK9	VSS			ge,			10515.6	8686.8
AL1	VSS			d ui.			17830.8	9601.2
AL11	VSS			Ue			8686.8	9601.2
AL14	VSS		· Wyle			Aefill.	5943.6	9601.2
AL2	VSS		269 0.			anno.	16916.4	9601.2
AL21	VSS	26	100		637	neo.	-457.2	9601.2
AL24	VSS	1 1100			dell		-3200.4	9601.2
AL27	VSS VSS	weg.			a uli		-5943.6	9601.2
AL3	VSS				tines.		16002	9601.2
AL30				inge			-8686.8	9601.2
AL36	VSS VSS			ed n.			-14173.2 15087.6	9601.2
AL4	VSS		10	ine				9601.2
7 01.			100%			defil	14173.2	9601.2
AM11	VSS VSS					4 Unice	8686.8 5943.6	10515.6 10515.6
AM14 AM17 AM19	VSS	32			e e	Wec.	3200.4	10515.6
AM17		1000			76		1371.6	10515.6
AM19	V55	::OeO			o Uli		13/1.6	10515.6
134	vss ndefined unde	Su,		efined und	Effines	Datash	eet, Volume	2 1 of 2
refined c	P		sined une			od nude,		



Table 9-1.

gen		۵	indefine			defined				ined un
	Pro	ocessor Land Inform	nation			unc		inte	J*)de	> *
		4 Uno			ndell.					
					July 1			Wes		
	Ta	ble 9-1. Proc	essor Land	List (Sheet	4 of 33)		ined.			
lefined u	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	ind
VOC	AM24	VSS	geilli			fines		-3200.4	10515.6	reg c
	AM27	VSS	VIII.			inge		-5943.6	10515.6	
	AM30	VSS				•		-8686.8	10515.6	1
	AM31	VSS			46/11/19			-9601.2	10515.6	1
	AM32	VSS			Uno			-10515.6	10515.6	1
	AM33	VSS		in ^e			6-	-11430	10515.6	1
	AM34	VSS		oge,			fine	-12344.4	10515.6	1
ined !	AM35	VSS		1011			"Was.	-13258.8	10515.6	1
Jefil.	AM36	VSS	- EINE			-0.0	37.	-14173.2	10515.6	7 11/1/
ILL	AM37	VSS	"Uge,			1efine		-15087.6	10515.6	eineo.
	AM38	VSS	9 01.			unar		-16002	10515.6	SI.,
	AM39	VSS				30		-16916.4	10515.6	
	AM40	VSS			46/11			-17830.8	10515.6	1
	AM5	VSS			und			14173.2	10515.6	1
	AN1	VSS		40	(e)O		-6	17830.8	11430	1
	AN10	VSS		9611			Silve	9601.2	11430	1
ed	AN11	VSS		4000			"uge	8686.8	11430	1
46fill.	AN14	VSS	0113			. 0	0.	5943.6	11430	70.0
nuc.	AN16	VSS	"VQe,			18 Fins		4114.8	11430	"veo
	AN19	VSS	90,			Inde		1371.6	11430	le,,,,
	AN22	VSS				eq.		-1371.6	11430	7
	AN23	VSS			defil			-2286	11430	1
	AN24	VSS			, uno			-3200.4	11430	1
	AN27	VSS		25.1	CO			-5943.6	11430	†
	AN30	VSS		76/			Fine	-8686.8	11430	†
, ced	AN36	VSS		4 11/10			ndell	-14173.2	11430	†
defill	AN4	VSS	275	(e _C			00 111	15087.6	11430	
Jundefines	AN5	VSS	"uqe _I "			defin		14173.2	11430	ined u
0.	AN6	VSS	9011			1109.6		13258.8	11430	deill.
	AN7	VSS	18-			veq n		12344.4	11430	
	AN8	VSS			4et			11430	11430	1
	AN9	VSS			, uno			10515.6	11430	1
	AP11	VSS		.*	vec.			8686.8	12344.4	1
	AP14	VSS		46			7/19-	5943.6	12344.4	1
08	AP24	VSS		4 Unio			"uge,	-3200.4	12344.4	1
46fills	AP27	VSS	c c	Ven			edu	-5943.6	12344.4	†
ed undefine	AP30	VSS	"Uge,			170	1	-8686.8	12344.4	ined
30	AP36	VSS	4 4 4 4			11098		-14173.2	12344.4	defill
·	Dat ad un	tasheet, Volume 1 of 2	2		ined unde	lived .	.e. 4	ned und	efined i	711-
	g un			INOIE						
113							4 nuc			
76/				40			20			



		undefine			adefined			
(intel				d undefined	Processor I	Land Infori	nation
				inger			defil	
	Ine			od or			nu _o	
Ta	ble 9-1. Prod	cessor Land	List (Sheet	5 of 33)				
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um
AP37	VSS	"uge,			4891170		-15087.6	12344
AP40	VSS	900			' nuo		-17830.8	12344
AP5	VSS			::0	30		14173.2	12344
AR1	VSS			delli			17830.8	13258
AR11	VSS			4 Ulus			8686.8	13258
AR14	VSS		27.5	SC			5943.6	13258
AR16	VSS		gen			Sine	4114.8	13258
AR17	VSS		9 011			11/06	3200.4	13258
AR18	VSS	2/3	0		_6	d	2286	13258
AR19	VSS	"Vge,			1efin		1371.6	13258
AR2	VSS	90,00			IIIO		16916.4	13258
AR20	VSS				60		457.2	13258
AR21	VSS			defil			-457.2	1325
AR24	VSS			uno			-3200.4	13258
AR27	VSS		45.	veo.			-5943.6	13258
AR3	VSS		461			Sill's	16002	1325
AR30	VSS		7 0100			1008	-8686.8	1325
AR31	VSS	eš.	Vec			99 711	-9601.2	1325
AR32	VSS	oge,			717		-10515.6	1325
AR33	VSS	4000			'lug'e'		-11430	1325
AR34	VSS	Wer.			-60 p.		-12344.4	1325
AR35	VSS			ie!			-13258.8	1325
AR36	VSS			Inou			-14173.2	1325
AR4	VSS			- CO			15087.6	1325
AR5	VSS		36			27:2	14173.2	1325
AT10	VSS		, uno			"QGI"	9601.2	1417
AT11	VSS		.0e0			-9.711.	8686.8	1417
AT12	VSS	79e,			(1)	80	7772.4	1417
AT13	VSS	70100			"UGE,		6858	1417
AT14	VSS	iller.			· veq n.		5943.6	1417
AT17	VSS			10	in		3200.4	1417
AT24	VSS			Inde			-3200.4	1417
AT25	VSS			· veg			-4114.8	1417
AT26	VSS		26			ci.	-5029.2	1417
AT27	VSS		7 11,00			~qeil	-5943.6	1417
AT28	VSS		ineo			971,	-6858	1417
AT29	VSS	-96			_8	1110	-7772.4	1417
AT30	vss und	4000		efined und	68	•	-8686.8	1417



Table 9-1.

gen			indefine			defined			£	ined un
	Pro	ocessor Land Inform	nation			une		inte	16,96	
		Inde			defill			HILL		
	0				Ulling			US OF		
	O Ta	ble 9-1. Proc	essor Land	List (Sheet	6 of 33)					
7 1/2	10	1.00		2.50 (3.11000	1	T	Non-	1		7
definec	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	interleaved (NIL)	X[um]	Y[um]	d und
	AT31	VSS	"uge.			4efill.		-9601.2	14173.2	iner.
_	AT32	VSS	, Or			Uno.		-10515.6	14173.2	
_	AT34	VSS			::00	0		-12344.4	14173.2	
_	AT36	VSS			gell.			-14173.2	14173.2	
_	AT37	VSS			Ulli			-15087.6	14173.2	
	AT38	VSS		ein ^e			69	-16002	14173.2	
_ \	AT39	VSS		vge,			iefile	-16916.4	14173.2	
"inea	AT40	VSS		701.			INO	-17830.8	14173.2	
delli	AT5	VSS	Sine					14173.2	14173.2	4 111/1
71/10	AT6	VSS	"Uge.			46/11		13258.8	14173.2	eineo.
	AT7	VSS	9 01			, uno		12344.4	14173.2	8///
	AT8	VSS				30		11430	14173.2	1
	AT9	VSS			4em			10515.6	14173.2	1
	AU1	VSS			7 0100			17830.8	15087.6	1
	AU25	VSS		610	G.		ó	-4114.8	15087.6	1
	AU30	VSS		gein			Sine	-8686.8	15087.6	
ed	AU34	VSS		4000			"uge	-12344.4	15087.6	
46fill.	AU4	VSS	013				0.00	15087.6	15087.6	nu ,
Uno.	AU5	VSS	'vge,			niigi		14173.2	15087.6	" ned
	AU7	VSS	90,			11000		12344.4	15087.6	eill
	AV2	VSS	5~			60		16916.4	16002	
-	AV26	VSS			Aeji!			-5029.2	16002	†
-	AV28	VSS			Uno			-6858	16002	†
-	AV30	VSS		.0.1	eq.			-8686.8	16002	1
-	AV34	VSS		46/1			Silve	-12344.4	16002	1
ed	AV38	VSS		7 11,00			Joe .	-16002	16002	1
iefilne.	AV5	VSS		60	1		9711.	14173.2	16002	-
INO	AV9	VSS	iuge _{III}			defill		10515.6	16002	ined v
Jundefines	AW3	VSS	7000			"Uge.		16002	16916.4	46411
	AW30	VSS	16.r			-60 n.		-8686.8	16916.4	
-	AW32	VSS			det			-10515.6	16916.4	†
	AW34	VSS			11100			-12344.4	16916.4	1
	AW36	VSS			Veg A			-14173.2	16916.4	1
	AW5	VSS		76,			715	14173.2	16916.4	1
0	AW9	VSS		4 1117010			adell.	10515.6	16916.4	+
Sing	AY27	VSS		CO.			-dulli-	-5943.6	17830.8	1
d undefine	AY30	VSS	indefi	(N *			180	-8686.8	17830.8	60
90	AY5	VSS				de,,	1	14173.2	17830.8	4efine
Ĺ		asheet, Volume 1 of 2	Nec.		ined unde	liusq n		ned und	ed l'	, ne
	4 OLL			"uge						
				eg ni.			11100			
				ine			9			



	intel	June			ed undefined			bn.	afined
1	intel					Processor	Land Infor	mation	
				"uger,			46/11		
6	ne			od ur			nuor		
Ta	ble 9-1. Proc	essor Land	List (Sheet	7 of 33)					
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	
AY7	VSS	"Jole !!!			ie filme		12344.4	17830.8	ane
AY9	VSS	9 01			IIIO		10515.6	17830.8	e _{ll}
B24	VSS				eq.		-3200.4	-16916.4	
B26	VSS			Yeili			-5029.2	-16916.4	
B28	VSS			4 nue			-6858	-16916.4	
B30	VSS		275	30.		e e	-8686.8	-16916.4	
B6	VSS		"ger			ight	13258.8	-16916.4	
C10	VSS		90,00			INO	9601.2	-16002	
C12	VSS	7/12	0			d	7772.4	-16002	
C14	VSS	"uge.			46/11		5943.6	-16002	(17)
C16	VSS	ed o			, nuc		4114.8	-16002	9e,
C18	VSS			c'a	ve _o		2286	-16002	
C20	VSS			"ge,			457.2	-16002	_
C22	VSS			og ni.			-1371.6	-16002	
C24	VSS			Nes			-3200.4	-16002	
C31	VSS		"uge.			Aefill.	-9601.2	-16002	_
C33	VSS		169 n.			4 Aluc	-11430	-16002	1
C35	VSS	il or			773	S _O ,	-13258.8 -15087.6	-16002	
C5 C5	VSS VSS	1000			odell.			-16002 -16002	1190
C8	VSS	ueo.			0,011,		14173.2 11430		JOE
D24	VSS				ine		-3200.4	-16002 -15087.6	
D24	VSS			· uge	1 *		-5029.2	-15087.6	_
D28	VSS			ed or	+		-6858	-15087.6	1
D30	VSS		76			77.3	-8686.8	-15087.6	1
D37	VSS		1 1100			"JOSI"	-15087.6	-15087.6	_
D39	VSS		ineo			39.411.	-16916.4	-15087.6	1
D4	VSS	"Uqe			105		15087.6	-15087.6	defi
D7	VSS	9 711.			ino		12344.4	-15087.6	dei
E11	VSS	Inc			ined.		8686.8	-14173.2	The same
E13	VSS			A	S		6858	-14173.2	1
E15	VSS			4 11100			5029.2	-14173.2	
E17	VSS			inec.			3200.4	-14173.2	
E19	VSS		~00	S		أأور	1371.6	-14173.2	
E21	VSS		-9 m			Mac	-457.2	-14173.2	
E23	VSS		ting			ed	-2286	-14173.2	
E3	VSS	und'			26		16002	-14173.2	
E31	VSS	eg n.			und		-9601.2	-14173.2	unde
138	ndefined unde			Jefined uni	Jefined		heet, Volum	ingine	
ed u	Ur.		4 und	Je.,		nde	ined u		



Table 9-1.

ger.			undefine		undefined	defined			Nije.
	Pro	ocessor Land Inforn	nation		eined	Une		inte	
		unci			delli				
	440			à	Ul.			No	
	o ^e Ta	ble 9-1. Proc	essor Land	6					
4 11					T		Non-		
definec	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	interleaved (NIL)	X[um]	Y[um]
	E33	VSS	"uge,			48/11.		-11430	-14173.2
	E35	VSS	0.			UNG		-13258.8	-14173.2
	E37	VSS			ine	O		-15087.6	-14173.2
	E6	VSS			gell.			13258.8	-14173.2
	E9	VSS			Ulli			10515.6	-14173.2
	F1	VSS		eine			60	17830.8	-13258.8
4.1	F10	VSS		"der			file	9601.2	-13258.8
"ineo	F22	VSS					Inos	-1371.6	-13258.8
Jeil.	F26	VSS	Silve			080	}	-5029.2	-13258.8
	F28	VSS	1000			46111		-6858	-13258.8
	F30	VSS	9 0.			, Uho		-8686.8	-13258.8
	F4	VSS				,0		15087.6	-13258.8
	F40	VSS			46 July			-17830.8	-13258.8
	F7	VSS			1 Olus			12344.4	-13258.8
	G11	VSS		013	30		60	8686.8	-12344.4
	G13	VSS		ger.			Sine	6858	-12344.4
· veg	G15	VSS		4 000			"Uge	5029.2	-12344.4
46fill.	G17	VSS	2013			.0	9.0.	3200.4	-12344.4
NUC.	G19	VSS	~9e,,			igin		1371.6	-12344.4
	G22	VSS	90,			Inde		-1371.6	-12344.4
	G3	VSS				eq.		16002	-12344.4
	G31	VSS			46 jil			-9601.2	-12344.4
	G33	VSS			Uno			-11430	-12344.4
	G6	VSS		.0.10	SQ.			13258.8	-12344.4
	H1	VSS		46/1			sine.	17830.8	-11430
-ec	H21	VSS		7 1140			100e1	-457.2	-11430
18fills	H24	VSS	225	60			79.711.	-3200.4	-11430
INO	H26	VSS	indet!!			defin		-5029.2	-11430
	H28	VSS	A Ulli			11096		-6858	-11430
	H30	VSS	ie.			60		-8686.8	-11430
	H35	VSS			Jeti			-13258.8	-11430
	H37	VSS			11000			-15087.6	-11430
	H39	VSS			690			-16916.4	-11430
	H4	VSS		76/			013	15087.6	-11430
0	H7	VSS		11100			oge,	12344.4	-11430
Gline	H9	VSS		veg ,			9 1111	10515.6	-11430
d undefine	J10	VSS	Yei			773	(8)	9601.2	-10515.6
3 0.	J12	VSS	7 0100			17981.		7772.4	-10515.6
, efin	Dat	: :asheet, Volume 1 of 2	2		ined under	lineq n		led und	rued nu
	-4 UL			inde				. *	
21/2				eg u.			" UING		
1611.			6	:10			<u> </u>		



	intel	3 unde			ed undefined			6	afined '
(intel)			iefin ^o		Processor	Land Infor	mation	
	4 1/11			INOP			defil		
130						۸	nuc		
Ta	ble 9-1. Proc	essor Land	List (Sheet	9 of 33)					
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	
J16	VSS	"Uger.			1efine		4114.8	-10515.6	"INEO
J18	VSS	900			INO		2286	-10515.6	e,,,
J20	VSS				180		457.2	-10515.6	
J3	VSS			Yelli			16002	-10515.6	
J32	VSS			4 1111			-10515.6	-10515.6	
J34	VSS		2/2	S		e.	-12344.4	-10515.6	
J6	VSS		yge,			ining	13258.8	-10515.6	
K1	VSS		900			INO	17830.8	-9601.2	
K14	VSS	7/19				20	5943.6	-9601.2	
K15	VSS	"uge			4efil.		5029.2	-9601.2	Silve
K17	VSS	ed v			I nug		3200.4	-9601.2	ger.
K19	VSS			4	ve _o		1371.6	-9601.2	
K22	VSS			ej.	,		-1371.6	-9601.2	
K24	VSS			A Ulli			-3200.4	-9601.2	
K26	VSS		6	Ver			-5029.2	-9601.2	
K28	VSS		oge,				-6858	-9601.2	
K30	VSS		9,00			no	-8686.8	-9601.2	
K33	VSS	i i e	100			ed	-11430	-9601.2	
K35	VSS	noo			defill		-13258.8	-9601.2	Silv
K37	VSS	ed			June		-15087.6		ye.
K39	VSS				inec.		-16916.4		
K4	VSS			196			15087.6	-9601.2	
K7	VSS			9 111.			12344.4	-9601.2	
L11	VSS			ino			8686.8	-8686.8	
L13	VSS		11000			Aefill	6858	-8686.8	
L32	VSS VSS		~69 v.			June	16002 -10515.6	-8686.8 -8686.8	_
L52	VSS	76				Lec.	13258.8	-8686.8	_
L9	VSS	4 0100			17961		10515.6	-8686.8	iefii ^r
M1	VSS 🐇	W _O			"Seg nii,		17830.8	-7772.4	Mon
M10	VSS	, N -			dine		9601.2	-7772.4	Ť
M12	VSS			lbni.			7772.4	-7772.4	1
M15	VSS			roeg or			5029.2	-7772.4	-
M17	VSS		2(2		c'a	3200.4	-7772.4	-
M19	VSS		7 1140.			~gell	1371.6	-7772.4	-
M21	VSS		ei Neo			29.711.	-457.2	-7772.4	1
M23	VSS	-9/				In	-2286	-7772.4	_
M25	VCC	7000			Inde		-4114.8		489
140	ndefined unde	fine		Jefined und	Jefined 2	Datasi	heet, Volum	Sine	under
zed u	Un		d und	Je.,		indef	ine		



Table 9-1.

Table 9-1. Processor Land List (Sheet 10 of 33) Land Land Name DDR3L LPDDR3 DDR4 Interleaved (IL) Interleaved (I	gen			indefine			-defined				ined un
Table 9-1. Processor Land List (Sheet 10 of 33) Land Name		Pro	ocessor Land Inform	nation			June		(inte		
Table 9-1. Processor Land List (Sheet 10 of 33) Land Name			, nuor			deill			1116		
Land Name		C				Julia			1170		
Land Land Name DDR31 LPDDR3 DDR4 Interleaved (IL) Interleaved (IL) V[un] V[u		o Ta	ble 9-1. Proc	essor Land	List (Sheet	10 of 33)		ed			
M27 VSS	-d u				'IUge	1		Non-			7
M27 VSS	Silver		Land Name	DDR3L	LPDDR3	DDR4		interleaved	X[um]	Y[um]	lon,
M29 VSS		M27	VCC	46(1),			sine C	(1122)	-5043.6	-7772 4	eg n.
M35 VSS				nu.			1961.				in
M37 VSS						0	Q.				1
M30 VSS			161			ighte	/			.0.	1
M4						11000			-111		1
M7 VSS								À	100		1
N3 VS5		AO.			76/11,			inec.	,		1
N33 VSS	ed ')A *			1000			-796/II			+
N6 VSS	4efine			ane				3			771
N8 VSS	INOIS			-ge _{ill}			FILLE				roeg o
P1 VSS		N8		1000			"Uge"				eilli
P35 VSS -13258.8 -5943.6 P37 VSS -15087.6 -5943.6 P39 VSS -16916.4 -5943.6 P4 VSS 15087.6 -5943.6 R3 VSS 16002 -5029.2 R3 VSS 11430 -5029.2 R6 VSS 13258.8 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS 13258.8 4114.8 T37 VSS 15087.6 -4114.8 T39 VSS 15087.6 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 15087.6 -4114.8 U3 VSS 11430 -3200.4 U4 VSS 13258.8 -2200.4 V1 VSS 17830.8 -2286 V37 VSS 15087.6 -2286 V39 VSS 1508			.0.	<u> </u>			90,				7
P37 VSS -15087.6 -5943.6 P39 VSS -16916.4 -5943.6 P4 VSS 15087.6 -5943.6 P4 VSS 15087.6 -5943.6 R3 VSS 16002 -5029.2 R33 VSS 11430 -5029.2 R6 VSS 11430 -5029.2 R7 VSS 11430 -5029.2 R8 VSS 11430 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T37 VSS 15087.6 -4114.8 T39 VSS 16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U3 VSS 11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V37 VSS 11430 -2286 V39 VSS 11430 -2286 V39 VSS 11430 -2286 W3 VSS 11430 -1371.6 W6 VSS 113258.8 -457.2			16/1			10,110	9			-0-	1
P39 VSS						inde					1
P4 VSS 15087.6 -5943.6 R3 VSS 16002 -5029.2 R33 VSS -11430 -5029.2 R6 VSS 13258.8 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS -13258.8 -4114.8 T37 VSS -15987.6 -4114.8 T39 VSS 15087.6 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 15087.6 -4114.8 U3 VSS 16002 -320.4 U33 VSS 13258.8 -320.4 V1 VSS 13258.8 -320.4 V1 VSS 13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -15087.6 -2286 V3 VSS -16916.4 -2286 V3 VSS -16916.4 -2286 V3 VSS -16916.4 -2286					0	60			447		1
R3 VSS 16002 -5029.2 R33 VSS -11430 -5029.2 R6 VSS 13258.8 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS -15087.6 -4114.8 T37 VSS 15087.6 -4114.8 T39 VSS 15087.6 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U3 VSS 13258.8 -3200.4 U1 VSS 17830.8 -2286 V35 17830.8 -2286 V35 17830.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -15087.6 -2286 W3 VSS -16916.4 -2286 W3 VSS -11430 -1371.6 W3 VSS -11430 -1371.6 W3 VSS -13258.8 -457.2		- 26			46/11			197113	J		1
R33 VSS -11430 -5029.2 R6 VSS 13258.8 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS -13258.8 -4114.8 T37 VSS -15087.6 -4114.8 T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS 16002 -3200.4 U5 VSS 17830.8 -2286 V35 17830.8 -2286 V35 175087.6 -2286 V35 175087.6 -2286 V37 VSS -15087.6 -2286 V39 VSS -15087.6 -2286 V8 VSS -16916.4 -2286 W3 VSS -11430 -1371.6 W3 VSS -11430 -1371.6 W3 VSS -13258.8 -457.2	ed	R3			1 11/10			VQC,			1
R6 VSS 13258.8 -5029.2 R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS -13258.8 -4114.8 T37 VSS -15087.6 -4114.8 T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS 13258.8 -3200.4 U4 VSS 17830.8 -2286 V35 VSS 17830.8 -2286 V35 15087.6 -2286 V37 VSS 11430 -2286 V39 VSS 11430 -2286 V8 VSS 11430 -2286 W3 VSS 11430 -1371.6 W3 VSS 13258.8 -1371.6 W6 VSS 13258.8 -457.2	iefine		VSS	.:.0	O			9711.	-11430		77.
R8 VSS 11430 -5029.2 T1 VSS 17830.8 -4114.8 T35 VSS -13258.8 -4114.8 T37 VSS -16916.4 -4114.8 T39 VSS 15087.6 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U3 VSS 16002 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V37 VSS -13258.8 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 11430 -1371.6 W3 VSS -11430 -1371.6 W6 VSS -13258.8 -1371.6 Y35 VSS -13258.8 -1371.6	INO			-9e;;;			FILLS		13258.8		red o
T1 VSS 17830.8 -4114.8 T35 VSS -13258.8 -4114.8 T37 VSS -15087.6 -4114.8 T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS 11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -15087.6 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 W3 VSS 11430 -2286 W3 VSS -11430 -1371.6 W6 VSS -11430 -1371.6 W6 VSS -13258.8 -1371.6 Y35 VSS -13258.8 -457.2		R8		700			1496.				eilli
T35 VSS -13258.8 -4114.8 T37 VSS -15087.6 -4114.8 T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U3 VSS -11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 W3 VSS 16002 -1371.6 W3 VSS -11430 -1371.6 W3 VSS -11430 -1371.6 W6 VSS -13258.8 -457.2			4	30			60				
T37 VSS -15087.6 -4114.8 T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS -11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W3 VSS -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS -13258.8 -457.2			10.1			10,11				-4114.8	1
T39 VSS -16916.4 -4114.8 T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS -11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W33 VSS -11430 -1371.6 W6 VSS 13258.8 -457.2						11000					1
T4 VSS 15087.6 -4114.8 U3 VSS 16002 -3200.4 U33 VSS -11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W3 VSS -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS -13258.8 -457.2						ed o			4(1)		1
U3 VSS 16002 -3200.4 U33 VSS -11430 -3200.4 U6 VSS 13258.8 -3200.4 V1 VSS 17830.8 -2286 V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W33 VSS -11430 -1371.6 W6 VSS 13258.8 -457.2		T4	,		76/			2013			1
V35 VSS V37 VSS V39 VSS V8 VSS W3 VSS W3 VSS W3 VSS W3 VSS W6 VSS Y35 VSS Y35 YSS Y35 YSS Y35 YSS Y35 YSS		D			1 1140			100e1			1
V35 VSS V37 VSS V39 VSS V8 VSS W3 VSS W3 VSS W3 VSS W3 VSS W6 VSS W6 VSS Y35 VSS -13258.8 -1371.6 Y35 VSS	18fills				(CO			29 m			1
V35 VSS V37 VSS V39 VSS V8 VSS W3 VSS W3 VSS W3 VSS W3 VSS W6 VSS W6 VSS Y35 VSS -13258.8 -1371.6 Y35 VSS	Uno	U6		"Gein		1	ni)				ined u
V35 VSS -13258.8 -2286 V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W3 VSS -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS -13258.8 -457.2		V1		-4011-			"IUGE"				defill
V37 VSS -15087.6 -2286 V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W33 VSS -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS -13258.8 -457.2				ler			697				10
V39 VSS -16916.4 -2286 V8 VSS 11430 -2286 W3 VSS 16002 -1371.6 W3 VSS -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS -13258.8 -457.2		V37	10.1			101				0_	†
V8 VSS W3 VSS W33 VSS W6 VSS Y35 VSS Y35 VSS Y35 VSS Y35 VSS						INO					†
W3 VSS W33 VSS H6002 -1371.6 -11430 -1371.6 W6 VSS 13258.8 -1371.6 Y35 VSS					. 4	CG .					†
W33 VSS W6 VSS Y35 VSS -13258.8 -1371.6 -13258.8 -457.2		W3	0.		76			2/13			†
W6 VSS Y35 VSS 13258.8 -1371.6 -13258.8 -457.2		7 //			4 1100			"UQEI,			†
Y35 VSS -13258.8 -457.2 Y37 VSS -15087.6 -457.2 Datasheet, Volume 1 of 2	46,111			ė.is	Ven			971.			†
Y37 VSS -15087.6 -457.2 Datasheet, Volume 1 of 2 141	, unos	Y35	VSS	~9e,	4b "		130	100			ed
Datasheet, Volume 1 of 2		Y37					"iuge"				Yelli,
adefinition and the second of		Dai	tasheet, Volume 1 of 2	Ure		Fined unde	Hined L	,0,0	ned und	efined 1	700
		9 n.			INO				*		
sing all the	713				red "			4 Unic			



Table 9-1.

		indefine			defined			
(intel	g o.		in in the	d undefined	Processor I	Land Infori	mation
	A Ultr			Inde.			defil	
			2013-1-1-1			6.	Ulli	
LINOTa	ble 9-1. Prod	cessor Land	List (Sheet	11 of 33)		tine		
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
Y5	VSS	"uge,			46/11/19		14173.2	-457.2
E40	VIDSOUT	900			unc		-17830.8	-14173.2
E38	VIDSCK				50		-16002	-14173.
E39	VIDALERT#			delli			-16916.4	-14173.2
U2	VCCST_PWRGD			A Ulli			16916.4	-3200.4
V5	VCCST		27/2	180			14173.2	-2286
АЈ9	VCCPLL_OC		"ger			iefino	10515.6	7772.4
V4	VccPLL		9011			illo	15087.6	-2286
AD5	VCCSA_SENSE	7/19-	0		_6	,0	14173.2	3200.4
AA6	VCCSA	"uge;			46/11/1		13258.8	457.2
AA7	VCCSA	od or			1100		12344.4	457.2
AB6	VCCSA				CO		13258.8	1371.6
AB7	VCCSA			defil			12344.4	1371.6
AB8	VCCSA			une			11430	1371.6
AC7	VCCSA			Vec.			12344.4	2286
AC8	VCCSA		deli			ni)	11430	2286
N7	VCCSA		4 000			"Uge,	12344.4	-6858
P7	VCCSA	611	Ven			eg 111	12344.4	-5943.6
R7	VCCSA	"gel			7113		12344.4	-5029.2
T7	VCCSA	4011			1100		12344.4	-4114.8
U7	VCCSA	Vien			-60		12344.4	-3200.4
V7	VCCSA			161			12344.4	-2286
W7	VCCSA			111100			12344.4	-1371.6
Y6	VCCSA			. red			13258.8	-457.2
Y7	VCCSA		26			27/2	12344.4	-457.2
Y8	VCCSA		, uno			"QGI"	11430	-457.2
AF4	VCCIO_SENSE		10e0			-9.711.	15087.6	5029.2
AJ23	VCCIO	~9e				180	-2286	7772.4
AK11	VCCIO	4000			"UGE,		8686.8	8686.8
AK14	VCCIO	Wer.			-co		5943.6	8686.8
AK24	VCCIO			10	ine		-3200.4	8686.8
M8	VCCIO			inde			11430	-7772.4
P8	VCCIO			ed v			11430	-5943.6
T8	VCCIO		20				11430	-4114.8
U8	VCCIO		' '//0,			adeil	11430	-3200.4
W8	VCCIO		::0e0			-4-1111	11430	-1371.6
F37	RSVD	76			2	Ins.	-15087.6	-13258.
F35	RSVD	10,00		efined und		· *	-13258.8	-13258.



Processor Land List (Sheet 12 of 33) Table 9-1.

efined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	4 110
,	G34	RSVD	"uge,			16/11/2		-12344.4	-12344.4	eineo.
	G35	RSVD	0.			, nuo		-13258.8	-12344.4	
	H33	RSVD			00	0		-11430	-11430	
	H34	RSVD			46/11			-12344.4	-11430	
	J33	RSVD			Ullia			-11430	-10515.6	
	J35	RSVD		cine			60	-13258.8	-10515.6	
	K32	RSVD		~ger.			igline	-10515.6	-9601.2	
" Vea	K34	RSVD		1011			INO	-12344.4	-9601.2	
defill	L31	RSVD	"ilue			-60		-9601.2	-8686.8	۷ د
	L33	RSVD	"Uge"			18/11/		-11430	-8686.8	eineo.
	M32	RSVD	900			1100		-10515.6	-7772.4	S.I
_	F39	VCCGT_SENSE			0	30		-16916.4	-13258.8	1
_	AA34	VCCGT			4eill.			-12344.4	457.2	1
	AA35	VCCGT			4 Uno			-13258.8	457.2	1
_	AA36	VCCGT		210	30		-6	-14173.2	457.2	1
	AA37	VCCGT		"Yeil			stine	-15087.6	457.2	1
· veg	AA38	VCCGT		A Un			"Uge,	-16002	457.2	1
46 ₁₁₁ ,	AB33	VCCGT	2013			0	9.7.	-11430	1371.6	1
Uo.	AB34	VCCGT	vqe,			i efine		-12344.4	1371.6	ined
	G36	VCCGT	90,00			11000		-14173.2	-12344.4	eill
	G37	VCCGT	3-			eo.		-15087.6	-12344.4	Ĭ
	G38	VCCGT			46/11			-16002	-12344.4	†
	G39	VCCGT			, una			-16916.4	-12344.4	†
_	G40	VCCGT		.0.10	e o			-17830.8	-12344.4	†
_	H36	VCCGT		46411	Y		sine.	-14173.2	-11430	1
e	H38	VCCGT		4 11/10			noe.	-16002	-11430	1
46/11/1	H40	VCCGT	27.5	60			9,711	-17830.8	-11430	1
IUO	J36	VCCGT	"Yejji			nin.		-14173.2	-10515.6	69
_	J37	VCCGT	40111			"Uge		-15087.6	-10515.6	AGLIII.
-	J38	VCCGT	le.			Seg n.		-16002	-10515.6	100
-	J39	VCCGT			det			-16916.4	-10515.6	†
-	J40	VCCGT			, unde			-17830.8	-10515.6	†
-	K36	VCCGT		A	ced o			-14173.2	-9601.2	†
	K38	VCCGT		76,	12		01:5	-16002	-9601.2	+
	K40	VCCGT		4 11/10/0			"yoen"	-17830.8	-9601.2	†
undefine	L34	VCCGT	A.	nea -			-9-711.	-12344.4	-8686.8	†
MOL	L35	VCCGT	, ndefi	, ,				-13258.8	-8686.8	_0
-	L36	VCCGT	4 400			ndefi!		-14173.2	-8686.8	18/1/10
Lefin ^e	Dat	asheet, Volume 1 of 2	2	ined unde	ined unde	ined W	ad undefil	<u> </u>	ed u	inc.
	4 010						ie fil			
				4 OII.						



			indefine			defined			
	(ntel)			ofine.	d undefined	Processor I	Land Infori	mation
		A COLOR			inuge.			defill	
	170			ال المام			6	OII.	
24	ОТа	ble 9-1. Proc	essor Land	List (Sheet	13 of 33)	T	Fine	,	
Iueo r	and #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um
l	L37	VCCGT	"Uge.			46/11		-15087.6	-8686.
L	L38	VCCGT	900			und		-16002	-8686
L	L39	VCCGT			.::0	50		-16916.4	-8686
L	L40	VCCGT			-ye,,,			-17830.8	-8686
N	433	VCCGT			4 Ullis			-11430	-7772
N	M34	VCCGT		2/2	800		e (-12344.4	-7772
<u> </u>	436	VCCGT		"ge,			efine	-14173.2	-7772
EINEO N	438	VCCGT		90,00			INO	-16002	-7772
N	140	VCCGT	7/7	U			O	-17830.8	-7772
N	N34	VCCGT	"uge			48/11/1		-12344.4	-685
N	N35	VCCGT	edu			und		-13258.8	-685
N	N36	VCCGT				CO.		-14173.2	-685
N	N37	VCCGT			4eil			-15087.6	-685
N	N38	VCCGT			A Ulli			-16002	-685
N	N39	VCCGT		¢\	Vec			-16916.4	-685
N ²	N40	VCCGT		age,			iefin	-17830.8	-685
"INED F	P33	VCCGT		ad un.			INO	-11430	-5943
F	P34	VCCGT	132	100			eq	-12344.4	-5943
F	P36	VCCGT	"uge"			46/11	•	-14173.2	-5943
F	P38	VCCGT	ed or			uno		-16002	-5943
F	P40	VCCGT				ve _O		-17830.8	-5943
F	R34	VCCGT			Jel.			-12344.4	-5029
F	R35	VCCGT			A Ullia			-13258.8	-5029
F	R36	VCCGT		6	ine			-14173.2	-5029
F	R37	VCCGT		~9e				-15087.6	-5029
C C	38	VCCGT		90,00			INOIS	-16002	-5029
Jelli F	R39	VCCGT	8	IUR			eq .	-16916.4	-5029
F	R40	VCCGT	inge			4611		-17830.8	-5029
٦	Т33	VCCGT	69 0			und		-11430	-4114
7	Т34	VCCGT	In			"Veo		-12344.4	-4114
٦	Т36	VCCGT			76			-14173.2	-4114
7	Т38	VCCGT			4 Ullin			-16002	-4114
	T40	VCCGT			einer			-17830.8	-4114
	J34	VCCGT		~96	3),		i)	-12344.4	-3200
6117	J35	VCCGT		od ni.			ina	-13258.8	-3200
gel, L	J36	VCCGT		ine			ed	-14173.2	-3200
ige, i	J37	VCCGT	100%	, "		10	11.	-15087.6	-3200
	J38	VCCGT	900		Jefined und	, Uho		-16002	-3200



Table 9-1.

ger.			indefine		undefined	defined			9	ine
	Pro	ocessor Land Inform	nation		. ned	und		inte	(8) 9(E)	
		inde			46 _{lll}			IIIIre		
		edu		7	nuc.			0611		
	76/1/						od u			
. 1/	о Та	ble 9-1. Proc	essor Land	List (Sheet	14 of 33)	T	in in the same			_
	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	
	U39	VCCGT	"uqe,			defile		-16916.4	-3200.4	
	U40	VCCGT	0.		,	Unc		-17830.8	-3200.4	3
	V33	VCCGT			ine)·		-11430	-2286	1
	V34	VCCGT			ye,			-12344.4	-2286	1
	V36	VCCGT			Ulli			-14173.2	-2286	Ī
	V38	VCCGT		eine,			eq.	-16002	-2286	Ī
	V40	VCCGT		gen			Silve	-17830.8	-2286	1
	W34	VCCGT	. (JULI			inde	-12344.4	-1371.6	1
eill.	W35	VCCGT	sine			-0.0		-13258.8	-1371.6	1
	W36	VCCGT	"Uger.			1efine		-14173.2	-1371.6	25.5
	W37	VCCGT	900			INGL		-15087.6	-1371.6	\$111
	W38	VCCGT				,O		-16002	-1371.6	Ī
	Y33	VCCGT			defill			-11430	-457.2	1
	Y34	VCCGT			uno			-12344.4	-457.2	1
	Y36	VCCGT		::08	,0		5-2	-14173.2	-457.2	1
	Y38	VCCGT		46/11			- fine	-16002	-457.2	1
	V6	VCCST		4 UNC			JOE!	13258.8	-2286	†
16/11/1	AJ24	RSVD	2013				9 71.	-3200.4	7772.4	1
	AJ25	RSVD	oge,,,			rine		-4114.8	7772.4	†
	AJ26	RSVD	7011			"luge"		-5029.2	7772.4	105
	AK21	RSVD	20			60 0.		-457.2	8686.8	4
	AJ27	RSVD			1etil			-5943.6	7772.4	+
	AJ28	RSVD			1100			-6858	7772.4	+
	AJ29	RSVD			eg. o.			-7772.4	7772.4	-
	AJ30	RSVD		76/11			ein ^e	-8686.8	7772.4	-
	AK27	RSVD		· Uno			oge,,,	-5943.6	8686.8	-
Gille	AT18	VDDQ		CO.			7 1111	2286	14173.2	+
	AT21	VDDQ	46 _{fll}	*		277	30	-457.2	14173.2	+
	AU13	VDDQ	7 0100			ndefil!		6858	15087.6	10
	AU15	VDDQ	(CO)			Seq ni.		5029.2	15087.6	400
	AU19	76/			ii)	762			15087.6	4
	AU23	VDDQ VDDQ			"uge,			1371.6		4
	AU23 AV11				ed n.			-2286 8686.8	15087.6	4
		VDDQ		i i	00				16002	4
	AV17	VDDQ		11996			Yelli,	3200.4	16002	4
	AV21	VDDQ		~69 m			4 nun	-457.2	16002	4
"uger.	AW10	VDDQ	101	11-		200	eo,	9601.2	16916.4	4
nuger.	AW14	VDDQ	11000			de'ill		5943.6	16916.4	4
	AW25	casheet, Volume 1 of 2	Weo.	6	ined undef	ined m.		-4114.8	16916.4	Jug.
	1 UU				*		ight	10		
				ed ni.			INGE			
16/11				ine			9,0			



ed undefined undefined Processor Land List (Sheet 15 of 33) Table 9-1.

			- ()					
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
AY12	VDDQ	"uge,			1efine		7772.4	17830.8
AY16	VDDQ	90			INUO		4114.8	17830.8
AY18	VDDQ			::0	30		2286	17830.8
AY23	VDDQ			delli			-2286	17830.8
C40	RSVD			4 Ullis			-17830.8	-16002
J19	RSVD		272	80			1371.6	-10515.6
B39	RSVD		"ge,			aefill.	-16916.4	-16916.4
J17	RSVD		og m.			INDO	3200.4	-10515.6
C38	VCC_SENSE	nig				O	-16002	-16002
A25	VCC	1000			deli		-4114.8	-17830.8
A26	VCC	ed			Julie		-5029.2	-17830.8
A27	VCC			***	ec		-5943.6	-17830.8
A28	VCC			uger.			-6858	-17830.8
A29	VCC			ed ui.			-7772.4	-17830.8
A30	VCC		(1)			.: 10	-8686.8	-17830.8
AJ11	VCC		11000			defill	8686.8	7772.4
AJ12	VCC		eg .			June	7772.4 6858	7772.4 7772.4
AJ13 AJ14	VCC	76 ⁽¹⁾			773	e.	5943.6	7772.4
AJ15	VCC	7 0100.			ye,		5029.2	7772.4
AJ16	VCC	ve _O			og m.		4114.8	7772.4
AJ17	VCC			i di	in a		3200.4	7772.4
AJ18	VCC			· inde			2286	7772.4
AJ19	VCC			eg c			1371.6	7772.4
AJ20	VCC		76,			7773	457.2	7772.4
AJ21	VCC		1 UNO.			"JOE"	-457.2	7772.4
AJ22	VCC	45	Weo.			~Q. 111.	-1371.6	7772.4
B25	VCC	79e3			17:0		-4114.8	-16916.4
B27	VCC	A UITT			"luge"		-5943.6	-16916.4
B29	VCC	lue.			600		-7772.4	-16916.4
B31	VCC			26			-9601.2	-16916.4
B32	VCC			una			-10515.6	-16916.4
B33	VCC			ined			-11430	-16916.4
B34	VCC		-96			li)	-12344.4	-16916.4
B35	VCC		4 University			"Wole"	-13258.8	-16916.4
B35 B36 B37 C25	VCC		ine.			ed b	-14173.2	-16916.4
B37	VCC	nde.			16		-15087.6	-16916.4
C25	VCC	39 D.			· nuo		-4114.8	-16002
146	vcc	fine		efined und	efineo	Datash 	neet, Volum	e 1 of 2
tefined U			ined uno			od undef		



Table 9-1.

gen			indefine			defined			
	Pro	ocessor Land Inforn	nation		undefined	unc		inte	3 9 8 7
		4 Uno.			"UGEI.			eill	
				60	OI.			il) a	
	o [©] Ta	ble 9-1. Proc	essor Land	List (Sheet	16 of 33)		ined.		
Jefined U	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
	C26	VCC	oge _{ill} ,			Singe		-5029.2	-16002
	C27	VCC	Oll I			"luge		-5943.6	-16002
	C28	VCC			.00	6		-6858	-16002
	C29	VCC			16/1/0			-7772.4	-16002
	C30	VCC			1110			-8686.8	-16002
	C32	VCC					λ.	-10515.6	-16002
	C34	VCC		46,111,			inec.	-12344.4	-16002
od'	C36	VCC		Uno.			-796/.	-14173.2	-16002
18fills	D25	VCC	ine)\(\)		_6	777.	-4114.8	-15087.6
	D27	VCC	-9e ₁₁₁			FILLS		-5943.6	-15087.6
	D29	VCC	A DICE			"Uge,		-7772.4	-15087.6
	D31	VCC	J.			90,0		-9601.2	-15087.6
	D32	VCC			1010	0		-10515.6	-15087.6
	D33	VCC			1000			-11430	-15087.6
	D34	VCC		-6	90.		3	-12344.4	-15087.6
	D35	VCC		18/11/1			::ne ⁰	-13258.8	-15087.6
	D36	VCC		11100			ge _{II} .	-14173.2	-15087.6
Silver	E24			9			7 1100	-3200.4	-14173.2
	E25	VCC	Aefill,			9773	O.	-3200.4	-14173.2
	E26	VCC	' AUC.			ygel.		-5029.2	-14173.2
			20			-0/1/1/			
	E27	VCC						-5943.6	-14173.2
	E28	VCC			"ge,			-6858	-14173.2
	E29	VCC			90,00			-7772.4	-14173.2
	E30	VCC		243				-8686.8	-14173.2
	E32	VCC		inge.			Aefill.	-10515.6	-14173.2
	E34	VCC		900			" Aluc.	-12344.4	-14173.2
undefine	E36	VCC	Ni s			0	20	-14173.2	-14173.2
I UII.	F23	VCC	1100			46/11		-2286	-13258.8
		VCC	ed			ullio		-3200.4	-13258.8
	F25	VCC			4	260		-4114.8	-13258.8
	F27	VCC			"ge,			-5943.6	-13258.8
	F29	VCC			4 111,			-7772.4	-13258.8
	F31	VCC		60	Ver			-9601.2	-13258.8
	F32	VCC		"vge,			inig	-10515.6	-13258.8
	F33	VCC		ad un.			Inor	-11430	-13258.8
egeri.	F34	VCC	Si .	Un			ed	-12344.4	-13258.8
d undefine	G23	VCC	uge.			4091	7	-2286	-12344.4
	G24	VCC	eg v.			und		-3200.4	-12344.4
	Dat ed un	tasheet, Volume 1 of 2	2		iined unde	ined		led und	efined U
	4 01			inde			Aefil	**	
21/2				ed n.			, hug-		
761				:100			~O		



ed undefined undefined Processor Land List (Sheet 17 of 33) Table 9-1.

California Cal		111.								
G26	defined		Land Name	DDR3L	LPDDR3	DDR4		interleaved	X[um]	Y[um]
G27 VCC	10.	G25	VCC	"uge,			46/11/10		-4114.8	-12344.4
G28 VCC		G26	VCC	90			, nuo		-5029.2	-12344.4
G29 VCC		G27	VCC				30		-5943.6	-12344.4
G30 VCC -8686 -632 VCC -10515 -122 VCC -1271		G28	VCC			yell.			-6858	-12344.4
G32 VCC		G29	VCC			4 Ullis			-7772.4	-12344.4
H22 VCC		AC			275	,20		-0	-8686.8	-12344.4
H23 VCC	۸.	G32			oge,			efin	-10515.6	-12344.4
H25 VCC	eineu	H22			900			Uno	-1371.6	-11430
H27 VCC	gel.			013				,O	-2286	-11430
H29 VCC				Mode			deilli		-4114.8	-11430
H31 VCC -9601 H32 VCC -10515 J21 VCC -457. J22 VCC -1371 J23 VCC -2286 J24 VCC -3200 J25 VCC -4114 J26 VCC -5943 J28 VCC -5943 J28 VCC -5943 J29 VCC -7772 J30 VCC -7772 J				ed			June		-5943.6	-11430
H32 VCC -10516 321 VCC -457. 322 VCC -1371 323 VCC -2286 324 VCC -2200 325 VCC -4114 326 VCC -5943 328 VCC -6856 331 VCC -6866 331 VCC -6866 331 VCC -6856 331 VCC -6856 321 VCC -6856 322 VCC -6856 331 VCC -6856 331 VCC -6856 331 VCC -6856 320 VCC -6856 321 VCC -6856 322 VCC -6856 331 VCC -6856 332 VCC -6856 331 VCC -6856 332			161	•			ler.		-7772.4	-11430
121 VCC						"ger.				-11430
132						ed ui.			- 4111	-11430
123 VCC	_		9	-	(1)	C.C.		:::08	U *	-10515.6
124 VCC		1 Dr.		-	11000	<u> </u>		defill		-10515.6
125	sine				reg			7 1100		-10515.6 -10515.6
126 VCC	"uge.			364			27/2	60,		-10515.6
127 VCC	_			4000			761,			-10515.6
J28 VCC	_			Ve _O			90,711.			-10515.6
129 VCC			76/			Ťa.	No.			-10515.6
330 VCC -8686 331 VCC -9601						- Inde			-7772.4	-10515.6
J31 VCC -9601						269.0			-8686.8	-10515.6
K16 VCC 4114. K18 VCC 2286 K20 VCC 457.2 K21 VCC -457. K23 VCC -2286 K25 VCC -4114 K27 VCC -5943 K29 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.			(O.		76,			7/3	-9601.2	-10515.6
K18 VCC 2286 K20 VCC 457.2 K21 VCC -457. K23 VCC -2286 K25 VCC -4114 K27 VCC -5943 K29 VCC -7772 K31 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.		7 0.			1 11/10			"Joje"	4114.8	-9601.2
K21 VCC -457. K23 VCC -2286 K25 VCC -4114 K27 VCC -5943 K29 VCC -7772 K31 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.	16fin				1000			29.711.	2286	-9601.2
K23 VCC -2286 K25 VCC -4114 K27 VCC -5943 K29 VCC -7772 K31 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.	nuo	K20	VCC	96,					457.2	-9601.2
K25 VCC -4114 K27 VCC -5943 K29 VCC -7772 K31 VCC -9601 L14 VCC 5943 L15 VCC 5029 L16 VCC 4114		K21	VCC	9011			inde		-457.2	-9601.2
K27 VCC -5943 K29 VCC -7772 K31 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.				Ine			60		-2286	-9601.2
K29 VCC -7772 K31 VCC 9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.	_	K25	VCC			76			-4114.8	-9601.2
K31 VCC -9601 L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.		K27	VCC			una			-5943.6	-9601.2
L14 VCC 5943. L15 VCC 5029. L16 VCC 4114.		K29	VCC			ined			-7772.4	-9601.2
L15 VCC 5029. L16 VCC 4114.		K31	VCC		-96			192	-9601.2	-9601.2
L15 VCC 5029. L16 VCC 4114. L17 VCC 3200. Datasheet, Vol		L14	VCC		4000			"LOGE"	5943.6	-8686.8
L16 VCC 4114. L17 VCC 3200. Datasheet, Vol	4efil	L15	VCC		ilues.			ed	5029.2	-8686.8
L17 VCC 3200. 148 Datasheet, Vol	nuc	L16	VCC	nde.			20		4114.8	-8686.8
148 Datasheet, Vol)	L17	VCC	eg or			uno		3200.4	-8686.8
4 a. Alamana de la companya de la co		148	ndefined unde	in a		efined und	efineo	Datasł	neet, Volum	e 1 of 2
te fine dunct	4efil	ued n	.*		sined uno			ad under	,,,,	

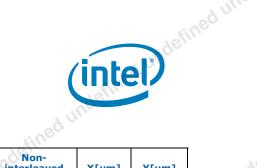


Table 9-1.

gerr			indefine			defined				ined une
	Dr	ocessor Land Inform	ation			Unc		inte	1.	
	FIC	ocessor Land Inform	iation		defille			IIILE		
		edu			nuc.			09611		
	46/11/	ble 0.1 Pres		Liet (Char) 10 of 22)		ed 1			
4 11	10 Ta	ible 9-1. Proc	essor Land	List (Sneet	18 01 33)	T	in in the second	1	1	7
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	d und
	L18	VCC	"uge			4efill.		2286	-8686.8	iner.
	L19	vcc	, O			nuc.		1371.6	-8686.8	
_	L20	VCC			ine.	0		457.2	-8686.8	
	L21	VCC			9eil.			-457.2	-8686.8	
_	L22	VCC			Ulli			-1371.6	-8686.8	
	L23	VCC		ein ^e			69	-2286	-8686.8	
_ \	L24	VCC		"ger.			efine	-3200.4	-8686.8	
"ineo	L25	VCC		Juli			inoc	-4114.8	-8686.8	
gen	L26	VCC	Sine			, ec		-5029.2	-8686.8	4 nu
	L27	VCC	"uge,			Aefill.		-5943.6	-8686.8	einec.
	L28	VCC	90.			, uno		-6858	-8686.8	8,,
	L29	VCC			0	8,0		-7772.4	-8686.8	
	L30	VCC			4elli.			-8686.8	-8686.8	
	M13	VCC			4 Ulli			6858	-7772.4	
	M14	VCC		202	C.		60	5943.6	-7772.4	
	M16	VCC		"ger.			iefine	4114.8	-7772.4	
ineo.	M18	VCC		900			INO	2286	-7772.4	
deilli	M20	VCC	Sin	0~			0	457.2	-7772.4	4 017
Ulu	M22	VCC	"uge			46/11		-1371.6	-7772.4	cineo.
	M24	VCC	900			unc		-3200.4	-7772.4	e,,
	M26	VCC				S _O		-5029.2	-7772.4	1
	M28	VCC			Yell			-6858	-7772.4	
	M30	VCC			4 Ullic			-8686.8	-7772.4	1
	AB38	RSVD		611	de C			-16002	1371.6	1
	AB37	RSVD		ger.			File	-15087.6	1371.6	
ine C	D11	THERMTRIP#		9 011			More	8686.8	-15087.6	
Jundefines	AU10	RSVD	113-	(Gr			600	9601.2	15087.6	20
Unc	J14	RSVD	"uqe _I "			16/11		5943.6	-10515.6	"ineo
<i>.</i>	AU9	RSVD	ed u.			, nuo		10515.6	15087.6	9ezz.
	J15	RSVD			. 6	760		5029.2	-10515.6	
	AB35	SKTOCC#			461			-13258.8	1371.6	1
	AB36	PROC_SELECT#			4 Une			-14173.2	1371.6	1
	K11	RSVD		e ²	Nen			8686.8	-9601.2	1
	D15	RSVD		~9e			Nigo:	5029.2	-15087.6	1
08	AC37	RSVD		4011			11000	-15087.6	2286	1
ed undefine	E7	RESET#	£.	Vez			ed	12344.4	-14173.2	
4 num	C39	PROCHOT#	"uge,			10:51		-16916.4	-16002	"ineo
SQ.	В9	PROC_PREQ#				Illos		10515.6	-16916.4	deill
	Dat	tasheet, Volume 1 of 2			ined unde	lived	4 undefi	ed und	efined 1)
	9 011			inde						
17/13				ed v.			4 Unes			
161,				ii No			20			



ed undefined undefined Processor Land List (Sheet 19 of 33) Table 9-1.

Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
B10	PROC_PRDY#	"Joe"			18 FIRE		9601.2	-16916.4
E8	PM_SYNC	900			INO		11430	-14173.2
D8	PM_DOWN			.:.0	30		11430	-15087.6
K8	RSVD_TP			delli			11430	-9601.2
L8	RSVD_TP			4 011			11430	-8686.8
J7	RSVD_TP		273	80.		e C	12344.4	-10515.6
18	RSVD_TP		"ge,			iefine	11430	-10515.6
K2	PEG_TXP[9]		9,000			Inos	16916.4	-9601.2
J1	PEG_TXP[8]	713				,O	17830.8	-10515.6
H2	PEG_TXP[7]	inde			4efill.		16916.4	-11430
G1	PEG_TXP[6]	69			unc		17830.8	-12344.4
F2	PEG_TXP[5]			44	'er		16916.4	-13258.8
E1	PEG_TXP[4]			gel.			17830.8	-14173.2
D2	PEG_TXP[3]			og ni.			16916.4	-15087.6
C3	PEG_TXP[2]		(4)	Ve		00	16002	-16002
T2	PEG_TXP[15]		"uge.			Jefill.	16916.4	-4114.8
R2	PEG_TXP[14]		·69 0.			T AUG.	16916.4	-5029.2
P2	PEG_TXP[13]	16			2773	e _O	16916.4	-5943.6
N1	PEG_TXP[12]	' AUC'			dell		17830.8 16916.4	-6858 -7772.4
M2	PEG_TXP[11]	Leo.			9/11/,		17830.8	-8686.8
L1 B4	PEG_TXP[10] PEG_TXP[1]			Ť	We a		15087.6	-16916.4
A5	PEG_TXP[0]			"uge,			14173.2	-17830.8
K3	PEG_TXN[9]			ed or			16002	-9601.2
J2	PEG_TXN[8]		76			27.5	16916.4	-10515.6
H3	PEG_TXN[7]		, uno			odell.	16002	-11430
G2	PEG_TXN[6]		veg .				16916.4	-12344.4
F3	PEG_TXN[5]	76,					16002	-13258.8
E2	PEG_TXN[4]	40100			"Uge,		16916.4	-14173.2
D3	PEG_TXN[3]	ILGO.			60 //		16002	-15087.6
C4	PEG_TXN[2]			10	ino		15087.6	-16002
T3	PEG_TXN[15]			illion			16002	-4114.8
R1	PEG_TXN[14]			ined			17830.8	-5029.2
P3	PEG_TXN[13]		. 69			132	16002	-5943.6
N2	PEG_TXN[12]		4 11/10			inge.	16916.4	-6858
M3	PEG_TXN[11]		i Leo			eg m	16002	-7772.4
UIO L2	PEG_TXN[10]				105	1100	16916.4	-8686.8
M3 L2 B5	PEG_TXN[1]	9,01			Illian		14173.2	-16916.4
150	PEG_TXN[1]	stine -	4	efined und	efineo	Datash	neet, Volum	 e 1 of 2
Jefined V			ined unc			od undef		



Processor Land List (Sheet 20 of 33) Table 9-1.

(qe)			indefine		undefined	defined			6	ine
	Pro	ocessor Land Inform	nation		ined	, Uluc,		inte	18, 9E	
		INOC			defili			IIIIce		
				Α	Ulue			1000		
	de Ta	ble 9-1. Proc	essor Land	List (Sheet :			ed l			
ال لم	Id	Die 9-1. Proc	essor Land	List (Slieet /	20 01 33)		18/10			7
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	
	A6	PEG_TXN[0]	"uge.			4efill.		13258.8	-17830.8	700
	L5	PEG_RXP[9]				und		14173.2	-8686.8	3
	K6	PEG_RXP[8]			ine	0		13258.8	-9601.2	
	J5	PEG_RXP[7]			gel.			14173.2	-10515.6	
	H6	PEG_RXP[6]			Ulli			13258.8	-11430	
	G5	PEG_RXP[5]		sine,			60	14173.2	-12344.4	
4.1	F6	PEG_RXP[4]		"ge"			fine	13258.8	-13258.8	1
"ineo	E5	PEG_RXP[3]		y our			Inos	14173.2	-14173.2]
gezz.	D6	PEG_RXP[2]	sine			200		13258.8	-15087.6	
	U5	PEG_RXP[15]	"uge"			461111		14173.2	-3200.4	cit
	Т6	PEG_RXP[14]	90.			· nue		13258.8	-4114.8	8,,
	R5	PEG_RXP[13]			0	3,0		14173.2	-5029.2	1
	P6	PEG_RXP[12]			4eili.			13258.8	-5943.6	1
	N5	PEG_RXP[11]			7 11110			14173.2	-6858	1
	M6	PEG_RXP[10]		ei ne	,0		-6	13258.8	-7772.4	Ī
	C7	PEG_RXP[1]		96gg			fine	12344.4	-16002	1
· veg	B8	PEG_RXP[0]		4 011			"UQ'E	11430	-16916.4	1
46.LIII.	L4	PEG_RXN[9]	277			- 0	9.0	15087.6	-8686.8	1
Ur.	K5	PEG_RXN[8]	"Ygeli.			i efine		14173.2	-9601.2	1
	J4	PEG_RXN[7]	900			Inde		15087.6	-10515.6	Je!
	H5	PEG_RXN[6]	<u> </u>			60		14173.2	-11430	
	G4	PEG_RXN[5]			46/11			15087.6	-12344.4	1
	F5	PEG_RXN[4]			1100			14173.2	-13258.8	1
	E4	PEG_RXN[3]			CQ.			15087.6	-14173.2	†
	D5	PEG_RXN[2]		46/11	*		Sills	14173.2	-15087.6	1
-00	U4	PEG_RXN[15]		' nuo			JOS.	15087.6	-3200.4	†
ndefined	T5	PEG_RXN[14]	225	(e _O			99.71	14173.2	-4114.8	†
10,0	R4	PEG_RXN[13]	- Geill,			defin	<u> </u>	15087.6	-5029.2	1
	P5	PEG_RXN[12]	4000			1496.		14173.2	-5943.6	146
	N4	PEG_RXN[11]	60.			260		15087.6	-6858	40
	M5	PEG_RXN[10]			Aeti			14173.2	-7772.4	1
	C6	PEG_RXN[1]			11000			13258.8	-16002	+
	B7	PEG_RXN[0]			069 A			12344.4	-16916.4	+
	L7	PEG_RCOMP		10/1	1.4-		775	12344.4	-8686.8	+
0	G7	PECI PECI		, 1170			~qej,,	12344.4	-12344.4	+
istine	W1	PCI_BCLKP		000			-0.411.5	17830.8	-1371.6	+
undefine	W2	PCI_BCLKN	- Ye _i	, ,		173	e.	16916.4	-1371.6	+
0.	F18	CFG[19]	1 0100			2961		2286	-13258.8	+
	Dat ed uni	asheet, Volume 1 of 2	5 Ween	į.	ined under	liveq n	d undefil	1	ed	700
	A UIV						16/1/	,,,		
				ed m.			INO			
16,111				ine			9			



Red undefined undefined

(intel			d undefine		Processor	Land Infor	mation
				1 UINC			"ge,	
10	ine					6-	OII.	
OTa	able 9-1. Proc	essor Land	List (Sheet	21 of 33)		FILE		
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um
F14	CFG[17]	deili			ie filne		5943.6	-13258
G18	CFG[18]	900			IIIO		2286	-1234
E14	CFG[16]				e _O		5943.6	-1417
M11	CFG_RCOMP			4efill			8686.8	-7772
E16	CFG[9]			, uno			4114.8	-1417
G16	CFG[8]		e5.0	150			4114.8	-1234
H20	CFG[7]		76,1			sine.	457.2	-1143
G21	CFG[6]		4 11/10			"Uge,	-457.2	-1234
H18	CFG[5]	27.5	S _Q			977	2286	-1143
F19	CFG[4]	gelli			Fin	V	1371.6	-1325
H16	CFG[3]	9011			"Uge		4114.8	-1143
F16	CFG[2]				60		4114.8	-1325
H19	CFG[15]			1011			1371.6	-1143
F21	CFG[14]			inde			-457.2	-1325
F20	CFG[13]			169.0			457.2	-1325
G20	CFG[12]		76/			2013	457.2	-1234
H17	CFG[11]		111100			oge,,,	3200.4	-114
F17	CFG[10]		veg.			70111	3200.4	-1325
F15	CFG[1]	76/1			77/2	80	5029.2	-1325
H15	CFG[0]	1000			"Yes,		5029.2	-1143
		160			-0111,			
H14 G14	BPM#[3]			-	We a		5943.6 5943.6	-114: -1234
	BPM#[2]			inge,				4/1/
D17	BPM#[1]			90,00			3200.4	-1508
D16	BPM#[0]			ine			4114.8	-1508
J11	RSVD		1000			Aefill'	8686.8	-1051
K13 J13 L12 K12	RSVD		-69 n.			nu.	6858	-9601
J13	RSVD		100			ea	6858	-1051
L12	RSVD	MOG			46/1		7772.4	-8686
	RSVD	aeg c			unc		7772.4	-9601
L10	RSVD	111			inea.		9601.2	-8686
K10	RSVD			296	14.		9601.2	-9601
H8	VSS			A Ullis			11430	-1143
AV39	RSVD_TP			iner			-16916.4	1600
AW38	RSVD_TP		290	S.,		ii	-16002	16916
AR22	VSS		9 01.			11000	-1371.6	13258
AR23	VSS		tine			eq.	-2286	13258
AT15	VSS	09	31		26		5029.2	14173
F9	EDP_TXP[3]			Jefined und	"IVOS		10515.6	-1325



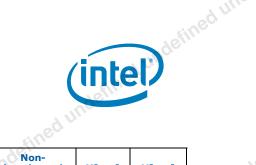
Table 9-1.

gen		_	indefine			undefined			£	ined un
	Pro	ocessor Land Inform	ation		ed	und		inte	1 s de	
		unde			defill			11116		
	0				Un			US.		
	o ^e Ta	ble 9-1. Proc	essor Land	List (Sheet	22 of 33)					
4 01	10			2.50 (5.11000	12 0. 00)		Non-		1	7
definec	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	interleaved (NIL)	X[um]	Y[um]	d und
	G10	EDP_TXP[2]	"uge.			46,111		9601.2	-12344.4	ineu
	D9	EDP_TXP[1]	0.			uno		10515.6	-15087.6	
	E10	EDP_TXP[0]			ine.	0		9601.2	-14173.2	
	G9	EDP_TXN[3]			geil.			10515.6	-12344.4	
	H10	EDP_TXN[2]			Ulli			9601.2	-11430	
	C9	EDP_TXN[1]		eine			d	10515.6	-16002	
2.0	D10	EDP_TXN[0]		"ger.			efine	9601.2	-15087.6	
sineo.	D14	EDP_DISP_UTIL					inoc	5943.6	-15087.6	
delli	D12	EDP_AUXP	Silve					7772.4	-15087.6	4 nu
	E12	EDP_AUXN	"uge			Aefill.		7772.4	-14173.2	einec.
	AU40	RSVD	9 0.			, une		-17830.8	15087.6	S
	AU39	RSVD			~::0	6,0		-16916.4	15087.6	
	M9	eDP_RCOMP			4e _{III}			10515.6	-7772.4	
	AF2	DMI_TXP[3]			A Ulling			16916.4	5029.2	
	AE2	DMI_TXP[2]		40			ed	16916.4	4114.8	
2	AD3	DMI_TXP[1]		"ger			istino	16002	3200.4	
"inec	AC2	DMI_TXP[0]		900			inos	16916.4	2286	
delli	AF3	DMI_TXN[3]	1919	0			d ·	16002	5029.2	4 01
UII.	AE1	DMI_TXN[2]	"UQIO			46111		17830.8	4114.8	"I'NEO"
_	AD2	DMI_TXN[1]	39 0			Uno		16916.4	3200.4	Ye.
<u>_</u>	AC1	DMI_TXN[0]			2.2	S _C ,		17830.8	2286	
<u>_</u>	AC4	DMI_RXP[3]			gel,	*		15087.6	2286	
<u>_</u>	AB4	DMI_RXP[2]			d ull			15087.6	1371.6	
<u>_</u>	AA4	DMI_RXP[1]		611	d _S			15087.6	457.2	<u> </u>
3	Y3	DMI_RXP[0]		yde.			4efill	16002	-457.2	<u> </u>
sine (AC5	DMI_RXN[3]		90,00			uno	14173.2	2286	<u> </u>
undefine	AB3	DMI_RXN[2]	iii			25.00	80	16002	1371.6	- A V
y on.	AA5	DMI_RXN[1]	"uqeili			defill		14173.2	457.2	FILES
_	Y4	DMI_RXN[0]	ed ~			ullo		15087.6	-457.2	ge.
<u> </u>	AG7	DDR1_DQSP[7]	▼		4	hea.		12344.4	5943.6]
<u> </u>	AL8	DDR1_DQSP[6]			"VGE,	. 7		11430	9601.2	1
-	AP8	DDR1_DQSP[5] / DDR1_DQSP[3] DDR1_DQSP[4] /			ueg ni.	DDR1_DQSP[5]	DDR1_DQSP[3]	11430	12344.4	
_	AN12	DDR1_DQSP[4] / DDR1_DQSP[2] DDR1_DQSP[3] /		inde ^f		DDR1_DQSP[4]	DDR1_DQSP[2]	7772.4	11430	
d undefine	AN28	DDR0_DQSP[7] DDR1_DQSP[2] /	£\	redu		DDR1_DQSP[3]	DDR0_DQSP[7]	-6858	11430	
d unc	AP33	DDR0_DQSP[6] ' DDR1_DQSP[1] /	"luge,			DDR1_DQSP[2]	DDR0_DQSP[6]	-11430	12344.4	FILEO
	AL33	DDR1_DQSP[1] / DDR0_DQSP[3]	ueg c		ined unde	DDR1_DQSP[1]	DDR0_DQSP[3]	-11430	9601.2	uge,
		"uge"			76				"ineu	
	Dat	casheet, Volume 1 of 2	<u>!</u>		, uno			~6	153	
								ed uli		
	ed un						dundefil	Jes		
				4 nus						
i efill				ineu			od u.			



led undefined undefined Table 9-1. Processor Land List (Sheet 23 of 33)

										=
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	und
O	AF35	DDR1_DQSP[0] / DDR0_DQSP[2]	undell			DDR1_DQSP[0]	DDR0_DQSP[2]	-13258.8	5029.2	ofined.
	AJ2	DDR0_DQSP[7] / DDR1_DQSP[5]	Ò			DDR0_DQSP[7]	DDR1_DQSP[5]	16916.4	7772.4	10.
	AN2	DDR0_DQSP[6] / DDR1_DQSP[4]			delif	DDR0_DQSP[6]	DDR1_DQSP[4]	16916.4	11430	-
	AU2	DDR0_DQSP[5] / DDR1_DQSP[1]			ed une	DDR0_DQSP[5]	DDR1_DQSP[1]	16916.4	15087.6	-
	AV7	DDR0_DQSP[4] / DDR1_DQSP[0]		adetin		DDR0_DQSP[4]	DDR1_DQSP[0]	12344.4	16002	-
Sineo	AV36	DDR0_DQSP[3] / DDR0_DQSP[5]	0	sq m.		DDR0_DQSP[3]	DDR0_DQSP[5]	-14173.2	16002	.0
ge.	AP38	DDR0_DQSP[2] / DDR0_DQSP[4]	ndefill			DDR0_DQSP[2]	DDR0_DQSP[4]	-16002	12344.4	"ined in
	AK38	DDR0_DQSP[1]	9,711			1100		-16002	8686.8	Jeill.
ŀ	AF38	DDR0_DQSP[0]				169		-16002	5029.2	
ŀ	AG6	DDR1_DQSN[7]			76/			13258.8	5943.6	1
ŀ	AM8	DDR1_DQSN[6]			11000			11430	10515.6	-
		DDR1_DQSN[5] /		45.1	veg .	DDR1_DQSN[5]		7 01,	13258.8	-
	AN12	DDR1_DQSN[3] DDR1_DQSN[4] /		indefi			DDR1_DQSN[3]	11430		
SUIS	AN13	DDR1_DQSN[2]		9,0,		DDR1_DQSN[4]	DDR1_DQSN[2]	6858	11430	
ugei	AN29	DDR1_DQSN[3] / DDR0_DQSN[7]	defi!	76		DDR1_DQSN[3]	DDR0_DQSN[7]	-7772.4	11430	ed ui
	AN33	DDR1_DQSN[2] / DDR0_DQSN[6]	ed une			DDR1_DQSN[2]	DDR0_DQSN[6]	-11430	11430	defille
	AK33	DDR1_DQSN[1] / DDR0_DQSN[3]				DDR1_DQSN[1]	DDR0_DQSN[3]	-11430	8686.8	
	AF34	DDR1_DQSN[0] / DDR0_DQSN[2]			unde	DDR1_DQSN[0]	DDR0_DQSN[2]	-12344.4	5029.2	
	АЈ3	DDR0_DQSN[7] / DDR1_DQSN[5]			ineo	DDR0_DQSN[7]	DDR1_DQSN[5]	16002	7772.4	
- 6	AN3	DDR0_DQSN[6] / DDR1_DQSN[4]		, unde		DDR0_DQSN[6]	DDR1_DQSN[4]	16002	11430	
defin	AU3	DDR0_DQSN[5] / DDR1_DQSN[1]		ineo.		DDR0_DQSN[5]	DDR1_DQSN[1]	16002	15087.6	30
711.0	AW7	DDR0_DQSN[4] / DDR1_DQSN[0]	4 nuge			DDR0_DQSN[4]	DDR1_DQSN[0]	12344.4	16916.4	18fineu
	AU36	DDR0_DQSN[3] / DDR0_DQSN[5]	Inec			DDR0_DQSN[3]	DDR0_DQSN[5]	-14173.2	15087.6	Inor
	AP39	DDR0_DQSN[2] / DDR0_DQSN[4]			bn.	DDR0_DQSN[2]	DDR0_DQSN[4]	-16916.4	12344.4	
	AK39	DDR0_DQSN[1]			69 0.			-16916.4	8686.8	1
ŀ	AF39	DDR0_DQSN[0]			line		4.4	-16916.4	5029.2	1
ŀ	AF6	DDR1_DQ[63]		009	-		Aeti	13258.8	5029.2	-
2/2	AE7	DDR1_DQ[62]		60 0.			, uno	12344.4	4114.8	-
"gell,	AH6	DDR1_DQ[61]	4.0	1100			neo .	13258.8	6858	A.
01.	AH7		inde	,		76		12344.4	6858	*inec
	154	DDR1_DQ[60]	finec		efined uni	Jefined unde	Datask	neet, Volum		undefined
,6.4				4 nuc			"uge			
1091	7 -						og u.			



ned undefined undefined at ? **Processor Land List (Sheet 24 of 33)** Table 9-1.

Jefined u	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	d und
	AF7	DDR1_DQ[59]	"uge.			48/11/1		12344.4	5029.2	ineo.
	AE6	DDR1_DQ[58]	V.			Und		13258.8	4114.8	
	AJ7	DDR1_DQ[57]			ine	0>		12344.4	7772.4	
	AJ6	DDR1_DQ[56]			ye,,,			13258.8	7772.4	
	AL6	DDR1_DQ[55]			Ulli			13258.8	9601.2	
	AM6	DDR1_DQ[54]		eine			, and	13258.8	10515.6	1
- 2/2	AL9	DDR1_DQ[53]		"uge.			defill.	10515.6	9601.2	1
FILL GO	AM9	DDR1_DQ[52]	00	70.			AUC	10515.6	10515.6	
ye.	AL7 AM7	DDR1_DQ[51]	46/11/2			SULE C		12344.4 12344.4	9601.2 10515.6	eg ui
-	AL10	DDR1_DQ[50] DDR1_DQ[49]	Uno.			"Yell,		9601.2	9601.2	Sine
-	AM10	DDR1_DQ[49]),			9 011.		9601.2	10515.6	
	AP6	DDR1_DQ[47] / DDR1_DQ[31]			defin	DDR1_DQ[47]	DDR1_DQ[31]	13258.8	12344.4	
	AR6	DDR1_DQ[46] / DDR1_DQ[30]			dun	DDR1_DQ[46]	DDR1_DQ[30]	13258.8	13258.8	1
9,	AP9	DDR1_DQ[45] / DDR1_DQ[29]		indefill		DDR1_DQ[45]	DDR1_DQ[29]	10515.6	12344.4	
defined	AR9	DDR1_DQ[44] / DDR1_DQ[28]	3013	d		DDR1_DQ[44]	DDR1_DQ[28]	10515.6	13258.8	
10.	AP7	DDR1_DQ[43] / DDR1_DQ[27]	"hyge"			DDR1_DQ[43]	DDR1_DQ[27]	12344.4	12344.4	Stilled
	AR7	DDR1_DQ[42] / DDR1_DQ[26]	,0		22.5	DDR1_DQ[42]	DDR1_DQ[26]	12344.4	13258.8	
	AR10	DDR1_DQ[41] / DDR1_DQ[25]			indefill	DDR1_DQ[41]	DDR1_DQ[25]	9601.2	13258.8	_
	AP10	DDR1_DQ[40] / DDR1_DQ[24] DDR1_DQ[39] /			ed or	DDR1_DQ[40]	DDR1_DQ[24]	9601.2	12344.4	_
	AL12	DDR1_DQ[23]		"indeili		DDR1_DQ[39]	DDR1_DQ[23]	7772.4	9601.2	_
define	AM12	DDR1_DQ[38] / DDR1_DQ[22]	2/3	edu		DDR1_DQ[38]	DDR1_DQ[22]	7772.4	10515.6	_
iuo	AP13	DDR1_DQ[37] / DDR1_DQ[21]	"Huge"			DDR1_DQ[37]	DDR1_DQ[21]	6858	12344.4	fined
	AR13	DDR1_DQ[36] / DDR1_DQ[20] DDR1_DQ[35] /	ed			DDR1_DQ[36]	DDR1_DQ[20]	6858	13258.8	ge.
	AL13	DDR1_DQ[19]			defi	DDR1_DQ[35]	DDR1_DQ[19]	6858	9601.2	_
	AM13	DDR1_DQ[34] / DDR1_DQ[18]			ed uli	DDR1_DQ[34]	DDR1_DQ[18]	6858	10515.6	_
	AP12	DDR1_DQ[33] / DDR1_DQ[17]		adefi	1.00	DDR1_DQ[33]	DDR1_DQ[17]	7772.4	12344.4	1
Stine	AR12	DDR1_DQ[32] / DDR1_DQ[16]	ά.	eq ui.		DDR1_DQ[32]	DDR1_DQ[16]	7772.4	13258.8	1
nuqetine,	AP28	DDR1_DQ[31] / DDR0_DQ[63]	indefi			DDR1_DQ[31]	DDR0_DQ[63]	-6858	12344.4	ined.
	AR28	DDR1_DQ[30] / DDR0_DQ[62]	ed ui.			DDR1_DQ[30]	DDR0_DQ[62]	-6858	13258.8	udetii
	Dat.	asheet, Volume 1 of 2	.		ined unde	lines		- 2	efined 1	
_{Leftin} s	Dat	issued, rounie 1 01 2			lined .		d undefil	red un	133	
ein ^e				ed nur.			' nuger.			



Red undefined undefined

AL28 AM28 AM28 AP29 AM29 AM29 AP31	Land Name B DDR1_DQ[29] / DDR0_DQ[61] B DDR1_DQ[28] / DDR0_DQ[60]	DDR3L	List (Sheet	25 of 33)	Interleaved	Non-	undefil		1
AL28 AM28 AR29 AP29 AM29	Land Name B DDR1_DQ[29] / DDR0_DQ[61] B DDR1_DQ[28] / DDR0_DQ[60] DDR1_DQ[27] /		unde	-			<u> </u>		1
# AL28 AM28 AR29 AP29 AM29	B DDR1_DQ[29] / DDR0_DQ[61] B DDR1_DQ[28] / DDR0_DQ[60] DDR1_DQ[27] /	DDR3L	LPDDR3	DDR4		Non-	1		
AM28 AR29 AP29 AM29	DDR0_DQ[61] DDR1_DQ[28] / DDR0_DQ[60] DDR1_DQ[27] /	d under		1	(IL)	interleaved (NIL)	X[um]	Y[um]	_
AR29 AP29 AM29	DDR0_DQ[60] DDR1_DQ[27] /	30			DDR1_DQ[29]	DDR0_DQ[61]	-6858	9601.2	Sineo
AP29		1		4.00	DDR1_DQ[28]	DDR0_DQ[60]	-6858	10515.6	
AM29				ndefil	DDR1_DQ[27]	DDR0_DQ[59]	-7772.4	13258.8	
AL29	DDR1_DQ[26] / DDR0_DQ[58]			ed or	DDR1_DQ[26]	DDR0_DQ[58]	-7772.4	12344.4	
	DDR1_DQ[25] / DDR0_DQ[57]		"ugeill		DDR1_DQ[25]	DDR0_DQ[57]	-7772.4	10515.6	
AP31	DDR1_DQ[24] / DDR0_DQ[56]	440	Sqn		DDR1_DQ[24]	DDR0_DQ[56]	-7772.4	9601.2	
	DDR1_DQ[23] / DDR0_DQ[55]	"Uqen			DDR1_DQ[23]	DDR0_DQ[55]	-9601.2	12344.4	sine
AN31	DDR1_DQ[22] / DDR0_DQ[54]	ed			DDR1_DQ[22]	DDR0_DQ[54]	-9601.2	11430	ger.
AP34	DDR1_DQ[21] / DDR0_DQ[53]			defi	DDR1_DQ[21]	DDR0_DQ[53]	-12344.4	12344.4	
AN34	DDR1_DQ[20] / DDR0_DQ[52]			ed unit	DDR1_DQ[20]	DDR0_DQ[52]	-12344.4	11430	
AP32	DDR1_DQ[19] / DDR0_DQ[51]		defi		DDR1_DQ[19]	DDR0_DQ[51]	-10515.6	12344.4	
AN32	DDR1_DQ[18] / DDR0_DQ[50]		ed un		DDR1_DQ[18]	DDR0_DQ[50]	-10515.6	11430	
AN35	DDR1_DQ[17] / DDR0_DQ[49]	adefi			DDR1_DQ[17]	DDR0_DQ[49]	-13258.8	11430	
AP35	DDR1_DQ[16] / DDR0_DQ[48]	sed un			DDR1_DQ[16]	DDR0_DQ[48]	-13258.8	12344.4	defille
AL31	DDR1_DQ[15] / DDR0_DQ[31]				DDR1_DQ[15]	DDR0_DQ[31]	-9601.2	9601.2	
AK31	DDR1_DQ[14] / DDR0_DQ[30]			4 unde	DDR1_DQ[14]	DDR0_DQ[30]	-9601.2	8686.8	1
AL34	DDR1_DQ[13] / DDR0_DQ[29]		10	ines	DDR1_DQ[13]	DDR0_DQ[29]	-12344.4	9601.2	1
AK34	DDR1_DQ[12] / DDR0_DQ[28]		-4 unas		DDR1_DQ[12]	DDR0_DQ[28]	-12344.4	8686.8	
AL32	DDR1_DQ[11] / DDR0_DQ[27]	46	Ine		DDR1_DQ[11]	DDR0_DQ[27]	-10515.6	9601.2	1
AK32	DDR1_DQ[10] / DDR0_DQ[26]	ad unos			DDR1_DQ[10]	DDR0_DQ[26]	-10515.6	8686.8	defin
AL35	DDR1_DQ[9] / DDR0_DQ[25]	ine			DDR1_DQ[9]	DDR0_DQ[25]	-13258.8	9601.2	Year
AK35	DDR1_DQ[8] / DDR0_DQ[24]			, und	DDR1_DQ[8]	DDR0_DQ[24]	-13258.8	8686.8	1
AH34	DDR1_DQ[7] / DDR0_DQ[23]			tined	DDR1_DQ[7]	DDR0_DQ[23]	-12344.4	6858	1
AG34	DDR1_DQ[6] / DDR0_DQ[22]		, und		DDR1_DQ[6]	DDR0_DQ[22]	-12344.4	5943.6	1
AE34	DDR1_DQ[5] / DDR0_DQ[21]		tinea		DDR1_DQ[5]	DDR0_DQ[21]	-12344.4	4114.8	
AE35	DDR1_DQ[4] / DDR0_DQ[20]	unde			DDR1_DQ[4]	DDR0_DQ[20]	-13258.8	4114.8	undefi
		eineo.		ı	ed niv	1		_	nuge
	bn.	SI			efine				,
1	.56			4 ung		Datasl	heet, Volume		
	DDR0_DQ[20]			efined und			ined in		
	n.		, und				11.		



Table 9-1.

gen			indefine			undefined			, S	lued nur
	Pro	ocessor Land Inform	ation		lefined	Tille		inte		
. 17	defii ⁿ	ble 9-1. Proc	essor Land				sined i	inge in		
defined b	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	und
	AH35	DDR1_DQ[3] / DDR0_DQ[19]	nuger.			DDR1_DQ[3]	DDR0_DQ[19]	-13258.8	6858	liveo
	AG35	DDR1_DQ[2] / DDR0_DQ[18]				DDR1_DQ[2]	DDR0_DQ[18]	-13258.8	5943.6	
-	AD35	DDR1_DQ[1] / DDR0_DQ[17]			adellin	DDR1_DQ[1]	DDR0_DQ[17]	-13258.8	3200.4	
-	AD34	DDR1_DQ[0] / DDR0_DQ[16]			dull	DDR1_DQ[0]	DDR0_DQ[16]	-12344.4	3200.4	†
. 1	AK1	DDR0_DQ[63] / DDR1_DQ[47]		ndefill		DDR0_DQ[63]	DDR1_DQ[47]	17830.8	8686.8	†
isfineo -	AH3	DDR0_DQ[62] / DDR1_DQ[46]	· ne	3.00		DDR0_DQ[62]	DDR1_DQ[46]	16002	6858	ind
inge	AK2	DDR0_DQ[61] / DDR1_DQ[45]	ndefill			DDR0_DQ[61]	DDR1_DQ[45]	16916.4	8686.8	aned u.
-	AH4	DDR0_DQ[60] / DDR1_DQ[44]	3			DDR0_DQ[60]	DDR1_DQ[44]	15087.6	6858	Silli
-	AH2	DDR0_DQ[59] / DDR1_DQ[43]			18/11/1	DDR0_DQ[59]	DDR1_DQ[43]	16916.4	6858	1
-	AK4	DDR0_DQ[58] / DDR1_DQ[42]			duna	DDR0_DQ[58]	DDR1_DQ[42]	15087.6	8686.8	1
-	AH1	DDR0_DQ[57] / DDR1_DQ[41]		46411		DDR0_DQ[57]	DDR1_DQ[41]	17830.8	6858	1
eined.	AK3	DDR0_DQ[56] / DDR1_DQ[40]		dunc		DDR0_DQ[56]	DDR1_DQ[40]	16002	8686.8	
indeili	AM1	DDR0_DQ[55] / DDR1_DQ[39]	defin			DDR0_DQ[55]	DDR1_DQ[39]	17830.8	10515.6	ed un
	AP1	DDR0_DQ[54] / DDR1_DQ[38]	d unc			DDR0_DQ[54]	DDR1_DQ[38]	17830.8	12344.4	efine
-	AM2	DDR0_DQ[53] / DDR1_DQ[37]			Vija.	DDR0_DQ[53]	DDR1_DQ[37]	16916.4	10515.6	
-	AP4	DDR0_DQ[52] / DDR1_DQ[36]			' nuge.	DDR0_DQ[52]	DDR1_DQ[36]	15087.6	12344.4	<u> </u>
-	AM3	DDR0_DQ[51] / DDR1_DQ[35]		1170	U.S.O.	DDR0_DQ[51]	DDR1_DQ[35]	16002	10515.6	<u> </u>
ed	AP3	DDR0_DQ[50] / DDR1_DQ[34]		4 nuge		DDR0_DQ[50]	DDR1_DQ[34]	16002	12344.4	_
undefined	AM4	DDR0_DQ[49] / DDR1_DQ[33]	iefil ^o	(OC)		DDR0_DQ[49]	DDR1_DQ[33]	15087.6	10515.6	الم
y m.	AP2	DDR0_DQ[48] / DDR1_DQ[32]	4 unde			DDR0_DQ[48]	DDR1_DQ[32]	16916.4	12344.4	defined
	AT3	DDR0_DQ[47] / DDR1_DQ[15]	C		a*a	DDR0_DQ[47]	DDR1_DQ[15]	16002	14173.2	
	AT4	DDR0_DQ[46] / DDR1_DQ[14]			indei	DDR0_DQ[46]	DDR1_DQ[14]	15087.6	14173.2	†
-	AW4	DDR0_DQ[45] / DDR1_DQ[13]		ď	ned b	DDR0_DQ[45]	DDR1_DQ[13]	15087.6	16916.4	†
-	AV3	DDR0_DQ[44] / DDR1_DQ[12]		Inde		DDR0_DQ[44]	DDR1_DQ[12]	16002	16002	†
define	AT2	DDR0_DQ[43] / DDR1_DQ[11]	si.	veg .		DDR0_DQ[43]	DDR1_DQ[11]	16916.4	14173.2	
ed undefine	AT1	DDR0_DQ[42] / DDR1_DQ[10]	' nuger			DDR0_DQ[42]	DDR1_DQ[10]	17830.8	14173.2	lefined.
	Dat	casheet, Volume 1 of 2	USC		ined unde	ined un	DDR1_DQ[10]	ind	efined L	hos
ı		ger.			fine			ueg r		
, efin	sq n.			ed nuo			, under			
76///				in			20			



Red undefined undefined

		intel			d undefine		Processor	Land Infor	mation	
. 1	Ta	ble 9-1. Proc	essor Land I	ist (Sheet	27 of 33)					
ined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	
	AV4	DDR0_DQ[41] / DDR1_DQ[9]	undell			DDR0_DQ[41]	DDR1_DQ[9]	15087.6	16002	Sined
_	AY4	DDR0_DQ[40] / DDR1_DQ[8]	Ö			DDR0_DQ[40]	DDR1_DQ[8]	15087.6	17830.8	30.
	AY6	DDR0_DQ[39] / DDR1_DQ[7]			adefin	DDR0_DQ[39]	DDR1_DQ[7]	13258.8	17830.8	
_	AW6	DDR0_DQ[38] / DDR1_DQ[6]			sq nii	DDR0_DQ[38]	DDR1_DQ[6]	13258.8	16916.4	
	AV8	DDR0_DQ[37] / DDR1_DQ[5]		ndefil		DDR0_DQ[37]	DDR1_DQ[5]	11430	16002	
IU60	AU8	DDR0_DQ[36] / DDR1_DQ[4]	0	sqm		DDR0_DQ[36]	DDR1_DQ[4]	11430	15087.6	
	AU6	DDR0_DQ[35] / DDR1_DQ[3]	ndefil			DDR0_DQ[35]	DDR1_DQ[3]	13258.8	15087.6	eined
	AV6	DDR0_DQ[34] / DDR1_DQ[2]	eg m			DDR0_DQ[34]	DDR1_DQ[2]	13258.8	16002	ger.
	AW8	DDR0_DQ[33] / DDR1_DQ[1]			Aefi	DDR0_DQ[33]	DDR1_DQ[1]	11430	16916.4	
	AY8	DDR0_DQ[32] / DDR1_DQ[0]			ed uno	DDR0_DQ[32]	DDR1_DQ[0]	11430	17830.8	
	AU35	DDR0_DQ[31] / DDR0_DQ[47]		Aefi		DDR0_DQ[31]	DDR0_DQ[47]	-13258.8	15087.6	
ine	AT35	DDR0_DQ[30] / DDR0_DQ[46]		ed nur		DDR0_DQ[30]	DDR0_DQ[46]	-13258.8	14173.2	
	AV37	DDR0_DQ[29] / DDR0_DQ[45]	defi			DDR0_DQ[29]	DDR0_DQ[45]	-15087.6	16002	-0.
	AU37	DDR0_DQ[28] / DDR0_DQ[44]	ed uno			DDR0_DQ[28]	DDR0_DQ[44]	-15087.6	15087.6	defiles
	AW35	DDR0_DQ[27] / DDR0_DQ[43]				DDR0_DQ[27]	DDR0_DQ[43]	-13258.8	16916.4	
	AV35	DDR0_DQ[26] / DDR0_DQ[42]			4 nuge	DDR0_DQ[26]	DDR0_DQ[42]	-13258.8	16002	
	AU38	DDR0_DQ[25] / DDR0_DQ[41]			ined	DDR0_DQ[25]	DDR0_DQ[41]	-16002	15087.6	
	AW37	DDR0_DQ[24] / DDR0_DQ[40]		A Unde		DDR0_DQ[24]	DDR0_DQ[40]	-15087.6	16916.4	
fine	AR40	DDR0_DQ[23] / DDR0_DQ[39]	10	luer		DDR0_DQ[23]	DDR0_DQ[39]	-17830.8	13258.8	ndefin
	AR39	DDR0_DQ[22] / DDR0_DQ[38]	d unos			DDR0_DQ[22]	DDR0_DQ[38]	-16916.4	13258.8	define
	AN37	DDR0_DQ[21] / DDR0_DQ[37]	luer			DDR0_DQ[21]	DDR0_DQ[37]	-15087.6	11430	Muc
	AN39	DDR0_DQ[20] / DDR0_DQ[36]			inde	DDR0_DQ[20]	DDR0_DQ[36]	-16916.4	11430	
	AR37	DDR0_DQ[19] / DDR0_DQ[35]			ined L	DDR0_DQ[19]	DDR0_DQ[35]	-15087.6	13258.8	
	AR38	DDR0_DQ[18] / DDR0_DQ[34]		indi		DDR0_DQ[18]	DDR0_DQ[34]	-16002	13258.8	
efir	AN40	DDR0_DQ[17] / DDR0_DQ[33]		ined		DDR0_DQ[17]	DDR0_DQ[33]	-17830.8	11430	
-	AN38	DDR0_D0[16] /	, unde			DDR0_DQ[16]	DDR0_DQ[32]	-16002	11430	Nijo.
_	158	DDR0_DQ[32]	Hines		efined und	Jefined III	Datas	heet, Volum	e 1 of 2	undefir
انانی ا	red u			ined und	No.		4 unde	111.		



Table 9-1.

dell			indefine			undefined			ę.	ined un
		ined			6-	nuo.			* 96	
	Pro	cessor Land Inform	nation		istined		(inte	217	
		od uli,			Inde			Je fill		
	nii)						44			
27.	Та	ble 9-1. Proc	essor Land	List (Sheet	28 of 33)		Finec			_
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	unds
	AL40	DDR0_DQ[15]	"uge.			48/11/1		-17830.8	9601.2	eineo.
	AL39	DDR0_DQ[14]			,	und		-16916.4	9601.2	
	AJ39	DDR0_DQ[13]			ine)		-16916.4	7772.4	
	AJ40	DDR0_DQ[12]			-gein.			-17830.8	7772.4	
	AL37	DDR0_DQ[11]			Ulli			-15087.6	9601.2	
	AL38	DDR0_DQ[10]		eine'			69	-16002	9601.2	
2 1	AJ37	DDR0_DQ[9]		"ger.			efine	-15087.6	7772.4	
"ineo	AJ38	DDR0_DQ[8]		9011			Inos	-16002	7772.4	5.
delli	AG40	DDR0_DQ[7]	Sine			200		-17830.8	5943.6	4 un
	AG39	DDR0_DQ[6]	"uge,			4efill.		-16916.4	5943.6	einer.
	AE40	DDR0_DQ[5]	9.00			, Und		-17830.8	4114.8	S
	AE39	DDR0_DQ[4]			.::0	,0		-16916.4	4114.8	1
	AG37	DDR0_DQ[3]			delli			-15087.6	5943.6	1
	AG38	DDR0_DQ[2]			4 Um			-16002	5943.6	1
	AE37	DDR0_DQ[1]		2013			6	-15087.6	4114.8	
	AE38	DDR0_DQ[0]		gen			istine	-16002	4114.8	
defineo	AL17	DDR1_WE#/ DDR1_CAB[2]/ DDR1_MA[14]	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]	- 0	d unos	3200.4	9601.2	1 110
nuc	AN18	DDR1_RAS# / DDR1_CAB[3]/ DDR1_MA[16]	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]	undefill		2286	11430	lefine o
	AL20	DDR1_PAR			0	S _O		457.2	9601.2	Ī
	AL15	DDR1_ODT[3]			46111			5029.2	9601.2	
	AP15	DDR1_ODT[2]			4 01/10			5029.2	12344.4	Ī
	AL16	DDR1_ODT[1]		273	CO			4114.8	9601.2	1
4	AM16	DDR1_ODT[0]		gen			Silve	4114.8	10515.6	Ī
Jundefines	AW27	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]		ed unde	-5943.6	16916.4	, u
3 une	AU26	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]	indefil		-5029.2	15087.6	defined
	AY26	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]	U.C.O.		-5029.2	17830.8	
	AW26	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]			-5029.2	16916.4	<u> </u>
ine!	AL23	DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]		indefin	-2286	9601.2	
ed undefine	AP23	DDR1_MA[4]	S.	Vez			ed	-2286	12344.4	4 /
4 nus	AM23	DDR1_MA[3]	"uge,			16/11		-2286	10515.6	sineo.
	Dat	asheet Volume 1 of 1	ined line		ined undef	lived nur		60	159	indefined l
Lefin ^s	מו	, sidile 1 01 2			lined .			red nur	-37	
isfin				ided nur			d under			



ted undefined undefined Processor Land List (Sheet 29 of 33) Table 9-1.

	1			.00	-				
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]
	AM22	DDR1_MA[2] / DDR1_CAB[5]/ DDR1_MA[2]	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]	undefine		-1371.6	10515.6
	AU28	DDR1_MA[15] / DDR1_CAA[8]/ DDR1_ACT#	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#	30		-6858	15087.6
	AY28	DDR1_MA[14] / DDR1_CAA[9]/ DDR1_BG[1]	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]			-6858	17830.8
ined	AR15	DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]		indefine	5029.2	13258.8
deili	AV27	DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]	4efine		-5943.6	16002
,	AU27	DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]	led nuc		-5943.6	15087.6
	AP18	DDR1_MA[10] / DDR1_CAB[7]/ DDR1_MA[10]	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]			2286	12344.4
	AL22	DDR1_MA[1] / DDR1_CAB[8]/ DDR1_MA[1]	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]		iefine	-1371.6	9601.2
define	AL19	DDR1_MA[0] / DDR1_CAB[9]/ DDR1_MA[0]	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]		ed moc	1371.6	9601.2
	AL26	DDR1_ECC[7]	"uge"			46/11	•	-5029.2	9601.2
	AL25	DDR1_ECC[6]	eg n.			und		-4114.8	9601.2
	AP25	DDR1_ECC[5]			47	ve _o		-4114.8	12344.4
	AP26	DDR1_ECC[4]			ger.			-5029.2	12344.4
_	AM25	DDR1_ECC[3]			od uli.			-4114.8	10515.6
	AM26	DDR1_ECC[2]			ine			-5029.2	10515.6
	AR26	DDR1_ECC[1]		"uge			defil!	-5029.2	13258.8
01/2	AR25	DDR1_ECC[0]		-eg (1			4 Aluc	-4114.8	13258.8
~0~	AN25 AN26	DDR1_DQSP[8] DDR1_DQSN[8]	76/	1111		6/1	vec,	-4114.8 -5029.2	11430 11430
	AM15		unos			ingle!			10515.6
_	AN17	DDR1_CS#[3] DDR1_CS#[2]	"UEO			90,711,		5029.2 3200.4	11430
	AN15	DDR1_CS#[1]	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\			ine		5029.2	11430
	AP17	DDR1_CS#[0]			· · · · · · · · · · · · · · · · · · ·			3200.4	12344.4
	AP19	DDR1_CKP[3]			TOEST TO			1371.6	12344.4
	AN20	DDR1_CKP[2]		26			£\(\)	457.2	11430
0	AP22	DDR1_CKP[1]		4 11/10/2			"vqe,	-1371.6	12344.4
46/1/1	AM20	DDR1_CKP[0]		:ineo			og m.	457.2	10515.6
undefire	AP20	DDR1_CKN[3]	~96	/			1110	457.2	12344.4
	AN21		29 010			11/98		-457.2	11430
	160	DDR1_CKN[2]	in .	. 6	efined und	efineo	Datash	neet, Volum	e 1 of 2
				ad um			inge		
16/11							9,0		



Table 9-1.

gem			undefine			undefined			Š	ined un
	Dro	ocessor Land Inform			ć _e o	Unc		inte	100	
	PIC	cessor Land Inform	iation		defille			IIILE		
				۸	Unc			10981		
	de ^{fill}	ble 9-1. Proc	essor I and	List (Sheet			ed l			
400	10	1100	C3301 Edild	List (Sirect			Non-			Ţ
definec	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	interleaved (NIL)	X[um]	Y[um]	d und
	AP21	DDR1_CKN[1]	"uge,			48/11.		-457.2	12344.4	inec
	AM21	DDR1_CKN[0]	,			UNO.		-457.2	10515.6	
	AU29	DDR1_CKE[3]			ine) ·		-7772.4	15087.6	
	AW29	DDR1_CKE[2]			-geill.			-7772.4	16916.4	
	AV29	DDR1_CKE[1]			Ulli			-7772.4	16002	
	AY29	DDR1_CKE[0]		eine,			69	-7772.4	17830.8	
ned V	AP16	DDR1_CAS#/ DDR1_CAB[1]/ DDR1_MA[15]	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]		indefine	4114.8	12344.4	
indefil.	AW28	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]	1. fined		-6858	16916.4	ined un
-	AM18	DDR1_BA[1] / DDR1_CAB[6]/ DDR1_BA[1]	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]	d unoc		2286	10515.6	3/11.
	AL18	DDR1_BA[0] / DDR1_CAB[4]/ DDR1_BA[0]	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]			2286	9601.2	
	AY25	DDR1_ALERT#		::09	,0			-4114.8	17830.8	<u> </u>
69	AV14	DDR0_WE#/ DDR0_CAB[2]/ DDR0_MA[14]	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]		ndefine	5943.6	16002	
undefine	AW13	DDR0_RAS# / DDR0_CAB[3]/ DDR0_MA[16]	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]	fine	3.311	6858	16916.4	ned un
-	AY15	DDR0_PAR	7 0/10			"uge"		5029.2	17830.8	efil.
	AY10	DDR0_ODT[3]	30.			60 ///		9601.2	17830.8	
-	AU12	DDR0_ODT[2]			Tito			7772.4	15087.6	<u> </u>
-	AU14	DDR0_ODT[1]			Inde			5943.6	15087.6	<u> </u>
-	AW11	DDR0_ODT[0]			eg .			8686.8	16916.4	<u> </u>
e d	AT22	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]		adefine	-1371.6	14173.2	
Jundefined	AT20	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]	ight	ed mil	457.2	14173.2	ined u
	AU21	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]	red nuge		-457.2	15087.6	defill
-	AV20	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]			457.2	16002	
-	AU20	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]		610	457.2	15087.6	
_0.	AT19	DDR0_MA[4]		7 1100			"Voel	1371.6	14173.2	†
46/11/2	AV19	DDR0_MA[3]	e S	Con			69 77.	1371.6	16002	
ed undefine	AU17	DDR0_MA[2] / DDR0_CAB[5]/ DDR0_MA[2]	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]	Indefil		3200.4	15087.6	defined
L		ndefi	Ines	ined under		liveg	od undefil	1	ined "	, inc
	₽≥+	asheet, Volume 1 of 2)		INGE			-8	161	
	Dat	asheet, volume 1 of 2	-					-y nuc	101	
Lefin ^r					(1)			Jes		
				4 nue			"uger.			
16/11/1				ineu			od ur.			



Red undefined undefined

	intel			id undefine		Processor I	Land Infor	ma
e.	ined			dulli		4	INGE	
	able 9-1. Proc	essor Land	List (Sheet	31 of 33)			undefin	
Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	
AU24	DDR0_MA[15] / DDR0_CAA[8]/ DDR0_ACT#	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#	undefine		-3200.4	:
AV23	DDR0_MA[14] / DDR0_CAA[9]/ DDR0_BG[1]	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]	90.		-2286	0
AV12	DDR0_MA[13] / DDR0_CAB[0] / DDR0_MA[13]	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]			7772.4	
AV22	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]		indefine	-1371.6	
AU22	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]	lefil ⁿ	,000	-1371.6	
AY14	DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]	led nuor		5943.6	:
AU18	DDR0_MA[1] / DDR0_CAB[8]/ DDR0_MA[1]	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]			2286	
AW15	DDR0_MA[0] / DDR0_CAB[9]/ DDR0_MA[0]	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]		Fine	5029.2	
AY31	DDR0_ECC[7]		7 11/10			"Uge,	-9601.2	
AW31	DDR0_ECC[6]	611	Ve _Q			ed m	-9601.2	
AV33	DDR0_ECC[5]	"ger			1173	•	-11430	
AU31	DDR0_ECC[4]	9/11/1			illge		-9601.2	
AV31	DDR0_ECC[3]	100			60		-9601.2	
AW33	DDR0_ECC[2]			461			-11430	c.
AT33	DDR0_ECC[1]			, uno			-11430	
AU33	DDR0_ECC[0]			ned			-11430	
AV32	DDR0_DQSP[8]		46			713	-10515.6	
AU32	DDR0_DQSN[8]		4 11/10			1000	-10515.6	
AV10	DDR0_CS#[3]	¢.	Uer.			69 77	9601.2	l
AV13	DDR0_CS#[2]	"Joje"			109		6858	
AU11	DDR0_CS#[1]	od W			Inde		8686.8	
AW12	DDR0_CS#[0]	Inc			: Neg		7772.4	
AT16	DDR0_CKP[3]			76			4114.8	
AW16	DDR0_CKP[2]			4 Ullio			4114.8	K
AW17	DDR0_CKP[1]			ined.			3200.4	
AW18	DDR0_CKP[0]		296			190	2286	
AU16	DDR0_CKN[3]		9011			inge	4114.8	
AV16	DDR0_CKN[2]		ines.			ed	4114.8	
AY17	DDR0_CKN[1]	100)*		10		3200.4	
AV18	DDR0_CKN[0]			efined und	ino		2286	



Processor Land List (Sheet 32 of 33) Table 9-1.

40.		bie 9-1. Proc	C3301 Land	List (Sifeet	J	1	ill's		ı	т
defined	Land #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um]	4 Uni
	AV25	DDR0_CKE[3]	"uge,			46/11/1		-4114.8	16002	ineo
	AV24	DDR0_CKE[2]	0.			nu _o .		-3200.4	16002	
	AW24	DDR0_CKE[1]			· ne	>		-3200.4	16916.4	1
	AY24	DDR0_CKE[0]			delli			-3200.4	17830.8	1
	AY11	DDR0_CAS#/ DDR0_CAB[1]/ DDR0_MA[15]	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]		, d	8686.8	17830.8	
aned V	AW23	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]		indefine	-2286	16916.4	
gein	AV15	DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]	defined		5029.2	16002	sined un
	AY13	DDR0_BA[0] / DDR0_CAB[4]/ DDR0_BA[0]	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]	d une		6858	17830.8	8,,,
	AT23	DDR0_ALERT#			delli			-2286	14173.2	
Ī	AC36	DDR_VTT_CNTL			4 1111			-14173.2	2286	
Ī	AC39	DDR1_VREF_DQ		410	300		6	-16916.4	2286	
	AC40	DDR0_VREF_DQ		"ger			iefine	-17830.8	2286]
ineo.	AB40	DDR_VREF_CA		9 01.			inos	-17830.8	1371.6	
deilli	AW2	RSVD_TP	1013				9	16916.4	16916.4	\ \ \
	AV1 C17 B16	RSVD_TP	1008			46/11/1		17830.8	16002	"INEO
		DDI3_TXP[3]	900			INING		3200.4	-16002	e,,
		DDI3_TXP[2]			20.00	So		4114.8	-16916.4	
Ī	C15	DDI3_TXP[1]			Aefil!			5029.2	-16002	1
	B14	DDI3_TXP[0]			4 11100			5943.6	-16916.4	1
	B17	DDI3_TXN[3]		275	er.		_	3200.4	-16916.4	1
4	A16	DDI3_TXN[2]		~gen.			Silve	4114.8	-17830.8	1
ine o	B15	DDI3_TXN[1]		-duis			inge	5029.2	-16916.4	1
gelli.	A14	DDI3_TXN[0]	113-	(e.c.			200	5943.6	-17830.8	4
inc	B11	DDI3_AUXP	"uge,			10/11/2		8686.8	-16916.4	"ineo
	C11	DDI3_AUXN	90,01			INO		8686.8	-16002	delli
	D20	DDI2_TXP[3]	100		4.4	eq.		457.2	-15087.6	
	C19	DDI2_TXP[2]			dell			1371.6	-16002	1
	D18	DDI2_TXP[1]			4 1/10			2286	-15087.6	1
	B18	DDI2_TXP[0]			Ueg.			2286	-16916.4	1
	E20	DDI2_TXN[3]		464			713-	457.2	-14173.2	1
	D19	DDI2_TXN[2]		AUNO			"Voe,	1371.6	-15087.6	1
undefine	E18	DDI2_TXN[1]	c c	Ver			eg m.	2286	-14173.2	1
UU0.	A18	DDI2_TXN[0]	"uqei,			1011		2286	-17830.8	t wed
	A12	DDI2_AUXP						7772.4	-17830.8	defill
1efin ^e		asheet, Volume 1 of 2	2	.4	ined under	ined	dundefil	ed und	efined U	,
	4 UL			inde			4efil	,		
				od ur.			INO			
7611.			6	ine			29			



ed undefined undefined

_ `	intel)			inine		Processor	Land Infor	mation
200	det m			d under			indefil	
Ta	ble 9-1. Proc	essor Land	List (Sheet	33 of 33)		eined		
and #	Land Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non- interleaved (NIL)	X[um]	Y[um
B12	DDI2_AUXN	"deti"			10 fine		7772.4	-16916
C23	DDI1_TXP[3]	9.00			INOL		-2286	-1600
B23	DDI1_TXP[2]			0	eg.		-2286	-16916
D22	DDI1_TXP[1]			Aetill.			-1371.6	-15087
C21	DDI1_TXP[0]			, uno			-457.2	-1600
D23	DDI1_TXN[3]		****	80			-2286	-1508
A23			Yell			sine'	-2286	-17830
E22			1 1100			2061,	-1371.6	-1417
D21		440	60			9711.		-1508
B13		- deilli			1113			-1691
		4 4100			"46,			-1600
		S _O			90,011			-1325
	16/			i i				-1691
				"uge"				-1508
				eg n.			400	-1325
						.:.06	U	-1325
ON.			11000			defill		
			69.0			4 9100		-114
		list.			273	S _C ,		-1234
		11000			ge _{III} .			-1325
		ed			un			-1143
	16/				ver.			-114
				"ge"				17830
G8				4 Ulli			11430	-1234
K9			C.	uec				-9601
J9			age,	*		Tilled		-1051
D13	CATERR#		900			ino	6858	-1508
W5	BCLKP	8	IUe			269	14173.2	-137
W4	BCLKN	inge.			461		15087.6	-137
U1	PROC_AUDIO_SD	ed or			, uno		17830.8	-3200
V2	DDOG AUDIO CDI	HOO					16916.4	-228
1/3	PROC_AUDIO_CLK			, unde			16002	-228
	C23 C23 C23 C23 C21 C23 C21 C23 C21 C23 C22 C21 C23 C23 C23 C22 C21 C23	DDI1_TXP[3] DDI1_TXP[2] DDI1_TXP[1] DDI1_TXP[0] DDI1_TXN[0] DDI1_TXN[2] DDI1_TXN[2] DDI1_TXN[1] DDI1_TXN[1] DDI1_TXN[0] DDI1_AUXP DDI1_AUXP DDI1_AUXP DDI1_AUXN F8 PROC_PWRGD B3 PROC_TRIGOUT D1 PROC_TRIGOUT D1 PROC_TRST# F13 PROC_TMS H13 PROC_TD0 G12 PROC_TD1 F11 PROC_TCK H12 RSVD_TP H11 RSVD_T	DDI1_TXP[3] DDI1_TXP[2] DDI1_TXP[0] DDI1_TXP[0] DDI3_DDI1_TXN[3] DDI1_TXN[2] DDI1_TXN[1] DDI1_TXN[1] DDI1_TXN[0] B3	DDI1_TXP[3] DDI1_TXP[2] DDI1_TXP[0] DDI1_TXP[0] DDI1_TXN[3] DDI1_TXN[3] DDI1_TXN[2] DDI1_TXN[1] DDI1_TXN[0] DDI1_TXN[0] DDI1_TXN[0] DDI1_TXN[0] DDI1_AUXP DDI1_AUXP DDI1_PROC_TRIGOUT DDI1_PROC_TRIGIN F12_PROC_TRST# F13_PROC_TMS H13_PROC_TD0 G12_PROC_TD1 F11_PROC_TCK H12_RSVD_TP H11_RSVD_TP AY3_VSS G8_VSS K9_CLK24P J9_CLK24N D13_CATERR# W5_BCLKP W4_BCLKN U1_PROC_AUDIO_SD O DDI1_TXN[1] DD	DDI1_TXP[3] DDI1_TXP[2] DDI1_TXP[1] DDI1_TXP[0] DDI3_DDI1_TXN[3] DDI1_TXN[3] DDI1_TXN[2] DDI1_TXN[1] DDI1_DDI1_TXN[0] DDI1_DDI1_TXN[0] DDI1_AUXP DDI1_AUXN FR PROCPWRGD B3 PROC_TRIGOUT D1 PROC_TRIGIN F12 PROC_TRST# F13 PROC_TOD G12 PROC_TDI F11 PROC_TCK H12 RSVD_TP H11 RSVD_TP AV3 VSS G8 VSS K9 CLK24P J9 CLK24N D1 PROC_AUDIO_SD O O D1 PROC	DDI2_AUXN DDI1_TXP[3] DDI1_TXP[2] DDI1_TXP[1] DDI1_TXP[0] DDI1_TXP[0] DDI1_TXN[0] DDI1_TXN[1] DDI1_TXN[1] DDI1_TXN[0] DDI1_TXN[0] DDI1_AUXP DDI1_AUXP DDI1_AUXN F8 PROCPWRGD B3 PROC_TRIGOUT D1 PROC_TRIGIN F12 PROC_TRST# F13 PROC_TMS H13 PROC_TDO D14 RSVD_TP H11 RSVD_TP H11 RSVD_TP H11 RSVD_TP H11 RSVD_TP H12 CALEAR# W5 BCLKP W4 BCLKN U1 PROC_AUDIO_SD O O O O O O O O O O O O O O O O O O O	STATE STAT	1312 DD12_AUXN 7772.4



	define defined	ed l'
	Introduction	define
	define ined (intel®	
A	under.	,
FILEC	ed III	
nde 1	Introduction	1
ed ui	1.1 Supported Technologies	3
IUG	1.1.1 Operating System Support	
	1.2.1 Processor Core Power Management	
	1.2.3 Memory Controller Power Management	
	1.2.4.1 Memory Power Savings Technologies	4
	1.2.4.2 Display Power Savings Technologies 1	4
	1.2.4.3 Graphics Core Power Savings Technologies	
dell	1.4 Package Support	
ed nii.	1.5 Processor Testability	5
	1.6 Terminology	
• ·	1.7 Related Documents	
2	Interfaces12.1System Memory Interface1	
	2.1.1 System Memory Technology Supported	
	2.1.1.1 DDR3L/-RS Supported Memory Modules and Devices2	0
	2.1.1.2 DDR4 Supported Memory Modules and Devices	
	2.1.2 System Memory Timing Support	1 2
defill	2.1.4 System Memory Frequency	3
4 Une	2.1.5 Technology Enhancements of Intel [®] Fast Memory Access	
	2.1.6 Data Scrambling 2 2.1.7 DDR I/O Interleaving 2	
fined undefine	2.1.8 Data Swapping	
	2.1.9 DRAM Clock Generation2	66
	2.1.10 DRAM Reference Voltage Generation	
	2.2 PCI Express* Graphics Interface (PEG)	
	2.2.2 PCI Express* Architecture	8
	2.2.3 PCI Express* Configuration Mechanism	
	2.2.4 PCI Express* Equalization Methodology	
uno	2.3.1 DMI Error Flow	
Jefined undefil	2.3.2 DMI Link Down3	0
Efil.	2.4 Processor Graphics	0
	2.4.1 API Support (Windows*)	
		1 4611.
	2.4.2.2 Hardware Accelerated Video Encode	
	2.4.2.3 Hardware Accelerated Video Processing	
		3
i a si	2.4.4 Switchable/Hybrid Graphics	
inde	2.4.5 GEN 9 Video Analytics	
ed n.	2.4.7 GT2 Graphics Frequency	5
efino	2.5 Display Interfaces	6
defined undefi	2.5.1 DisplayPort*	U O
	2.5.2 High-Definition Multified a Interface (HDMI*)	1 10
	2.5.4 embedded DisplayPort* (eDP*)	1 11000
	2.5 Display Interfaces	
Date 1	act Adums 1 of 2	1
Datash	eet, Volume 1 of 2	1
	ineo cineo	
ed n.	" Thos	
efine	ined and all the second	



	hed und	Hine	fined undefined s	ad undefined v	ned u
	ed une		4 under		ndefill.
(inte			ined	ned v	
7 111		unde		defill	
4efine				od ume	
INDO		rated Audiople Display Configurations (I		41	
		ple Display Configurations (S			
	2.5.8 High-	Bandwidth Digital Content F	Protection (HDCP)	43	
	2.5.9 Displa	ay Link Data Rate Support		44	ed
		ay Bit Per Pixel (BPP) Suppo ay Resolution per Link Width			
2.6		ironmental Control Interface			
2.0		Bus Architecture			
3 Tech		d			
3.1	Intel [®] Virtual	ization Technology (Intel® \	/T)	48	
delli	3.1.1 Intel [®]	[®] Virtualization Technology	(Intel [®] VT) for IA-32, In	tel [®] 64 and Intel [®]	
dune	Archit	tecture (Intel® VT-X)	(T + 18) (T) (48	3
3.2	3.1.2 Intel®	[®] Virtualization Technology (nnologies	(Intel® VI) for Directed	دع 1/0 (Intel® ۸۱-q)50) }
3.2	3.2.1 Intel [®]	® Trusted Execution Technol	loav (Intel® TXT)	53	, }
	3.2.2 Intel®	R Advanced Encryption Stan	dard New Instructions (I	Intel [®] AES-NI)54	inec
	3.2.3 PCLM	ULQDQ (Perform Carry-Less	s Multiplication Quad wor	rd) Instruction54	46 July
		[®] Secure Key			
		ute Disable Bit Guard Technology			
21	3.2.7 Supe	rvisor Mode Execution Prote	ction (SMFP)	5c) -
		Supervisor Mode Access Pro			
dell	3.2.9 Intel [®]	[®] Memory Protection Extens	sions (Intel® MPX)	55)
A Ullie	3.2.10 Intel [®]	Software Guard Extension	s (Intel [®] SGX)	56	•
410 ⁶⁰		[®] Virtualization Technology (erformance Technologies			
3.3		Brothlance reclinologies Byper-Threading Technolo			
	3.3.2 Intel®	[®] Turbo Boost Technology 2	.0	57	· · · · · · · · · · · · · · · · · · ·
	3.3.2	.1 Intel [®] Turbo Boost Tecl	hnology 2.0 Frequency	57	46,1,
		Advanced Vector Extension			
		$^{\mathbb{R}}$ 64 Architecture x2APIC r Aware Interrupt Routing (I			
6-	3.3.6 Intel [®]	B Transactional Synchroniza			
3.4	Intel [®] Image	Signal Processor (Intel® IS	5P)	60)
	3.4.1 Platfo	orm Imaging Infrastructure		60)
3.5	Debug Techn	ologies		61	-
	3.5.1 Intel®	Processor Trace			
3.4 3.5 4 Pow 4.1 4.2	er Manageme	nt		62	<u>)</u> -
4.1 4.2	Advanced Co	nfiguration and Power Interf Core Power Management			
4.2		W controlled P-states			
	4.2.1	.1 Enhanced Intel [®] Speed	Step [®] Technology	66	4 m.
		.2 Intel [®] Speed Shift Tech	nnology	67	6
		Power Idle States			
istino		esting Low-Power Idle State essor IA core C-State Rules			
		age C-States			
ed n.	4.2.6 Packa	age C-States and Display Re	esolutions	73	}
4.3		emory Controller (IMC) Pow		74	
196		oling Unused System Memor 1 Power Management and Ir		74	<u> </u>
ndefined undefine		1 Initialization Pole of CK	E	74 	1130
	4.3.2	.2 Conditional Self-Refresh	h	76	I nuge.
2 Jefined undefine	4 nuger.	.2 Conditional Self-Refresh	ndefine	ie fil	led undefil
2			7.	Datasheet, Volume 1 of 2	2
den		Sine		ined.	
4 Une		"uge"		defil.	
		og n.		· IIno-	
16,111					



	define	fined		sed un
Fined undefined und	raed ulli	namid Rever Down	def	
nd	efil.	18 inec	(intel)	
ned uli		d unoc	in effi	
defill	4.3.2.3 Dvn	namic Power-Down	76	
ad une	4.3.2.4 DRA	AM I/O Power Management	<i></i> 76	
	4.3.3 DDR Electrica 4.3.4 Power Trainin	l Power Gating (EPG)g		
4.4	PCI Express* Power N	Nanagement	77	edi
4.5 4.6		e (DMI) Power Management ower Management		Kill.
4.0	4.6.1 Memory Powe	er Savings Technologies	77	
		el [®] Rapid Memory Power Management (Intel [®] Smart 2D Display Technology (Intel [®] S		
ed u.	4.6.2 Display Power	r Savings Technologies	78	
4efine	4.6.2.1 Inte	el® (Seamless & Static) Display Refresh Ra	te Switching (DRRS)	
unoc	4.6.2.2 Inte	n eDP* Portel [®] Automatic Display Brightness		
	4.6.2.3 Smc	ooth Brightnessl [®] Display Power Saving Technology (Intel		
	4.6.2.5 Low	r-Power Single Pipe (LPSP)	79	λ
	4.6.3 Processor Gra	aphics Core Power Savings Technologies	79	
	4.6.3.1 Inte 4.6.3.2 Inte	el [®] Graphics Dynamic Frequency el [®] Graphics Render Standby Technology (1		e,
4.7	4.6.3.3 Dyn	amic FPS (DFPS)	79	
4.7				
5 The : 5.1		anagement		
ndell 3.1		siderations		
ed ni.	5.1.2 Intel® Turbo I	Boost Technology 2.0 Power Monitoring	82	
efine		Boost Technology 2.0 Power Control kage Power Control		
	5.1.3.2 Plat	form Power Control	83	
		bo Time Parameter (Tau) TDP (cTDP) and Low-Power Mode		16fills
	5.1.4.1 Con	figurable TDP	84	
defined undefined i	5.1.4.2 Low 5.1.5 Thermal Mana	r-Power Modeagement Features		
ed !	5.1.5.1 Ada	ptive Thermal Monitor	85	
	5.1.5.2 Digi 5.1.5.3 PRO	tal Thermal Sensor CHOT# Signal		
, unoc	5.1.5.4 Bi-D	Directional PROCHOT#	89	
	5.1.5.5 Volt 5.1.5.6 The	age Regulator Protection using PROCHOT# rmal Solution Design and PROCHOT# Beha		
deill	5.1.5.7 Low	-Power States and PROCHOT# Behavior	90	
	5.1.5.8 THE 5.1.5.9 Criti	RMTRIP# Signalical Temperature Detection		
	3.1.3.10 011	Demand Mode R Based On-Demand Mode	90	19e.
	5.1.5.12 I/O	Emulation-Based On-Demand Mode	91	
A		ry Thermal Management		
5.2		gn Power (SDP)rmal and Power Specifications		
"uge,"	5.2.1 Thermal Profil	le for PCG 2015D Processor	95	
ed u.		le for PCG 2015C Processorle for PCG 2015B Processor	0.7	
define	5.2.4 Thermal Profi	le for PCG 2015A Processor	98	
defined under 5.2	5.2.5 Thermal Metro	ology	99	
6 Sign	nal Description	for a supplier of the supplier	100	defill
6.1	System Memory Inter	face	101	111
	IIIUGE	adefili.	Fineu	
Datasheet, Vo	olume 1 of 2	facedefined undefine		
Datasneet, Vo		Hines	rued n.	
dune		inge.	defille	
diner		sed v	unc	



		define	4efined		eined u
(intel		undefined undefined		d undefined u
		. 1	nuger.	defin	
46			ıls	ed un	104
4 Uno	6.2 PCI Expres	os crapinos (i Ec) oigila	ls		104
	6.4 Reset and	Miscellaneous Signals			105
	6.5 embedded	DisplayPort* (eDP*) Sig	nals		106
	6.6 Display Int	Clocking Signals			107
			ıls		
			to Function (NCTF) Signa		
	6.13 Processor	Internal Pull-Up/Pull-Dov	vn Terminations		111
7	Electrical Speci	fications			112
	7.1 Processor	Power Rails			112
111.					
	7.1.2 V _C 7.2 DC Specifi	$\mathcal C$ voltage Identification (VID)	C	112
			Specifications		
	7.3	2.1.1 Vcc DC Specificat	ions		113
	-0	2 4 2 VDDO DC C:6'-	cationscations		446
	7	2.1.4 VccSA DC Specific	cations		117
fined und	1 7	2.1.5 VccIO DC Specific	cations		117
	7 7	2.1.6 VCCST DC Specific 2.1.7 VccPLL DC Specific	cations		118
9 011.	7.2.2 Pro	ocessor Interfaces DC Sp	ecifications	76/	119
RINGS	7.:	2.2.1 DDR3L/-RS DC S	pecifications		119
3°	7 7.:	2.2.2 DDR4 DC Specific 2.2.3 PCI Express* Gra	phics (PEG) DC Specificat	tions	120
	7	2.2.4 Digital Display In	terface (DDI) DC Specific	ations	122
	7.0	2.2.5 embedded Displa	yPort* (eDP*) DC Specific	cation	122
	7.	2.2.7 GTL and OD DC S	Specifications		123
	June 7.1	2.2.8 PECI DC Characte	eristics		124
8	Package Mecha	nical Specifications			125
	8.1 Package M	lechanical Attributes	?		125
4 111	8.2 Package S	torage Specifications			126
siven a	Processor Land	Information			. 127
ej,		stine	4.4		
			defil		
		da	, uno		dell
	ie film				ed uli.
	IIIO		defill		
			4 Unic	ind ⁶	
	16till			od un	
<i>\(\text{\text{U}}\)</i>		delli			
ined.		4 ulli			
46ill.				edu	
		ader.	101	Illia	
		of m.	Inde		defil
			edu		4 nuc
	ade.		18fin		
Δ	ad un.		Inoc	Datasheet Volume	1 of 2
+	sine			Datasneet, volume	- VI 2
		101	11.	ineo.	
291		Inois		egen.	
Stille		ined to	cations cation	dun	
3.67					



	define		sined .		ed v
	1-1 S-Processor Line Plat 1-2 Merged XDP Connect 2-1 Intel [®] Flex Memory T 2-2 Interleave (IL) and N 2-3 PCI Express* Related	forms stined undestine	, unde.		defills
	define			(intel)	
	d une	inder			
iefine		ined t		od une	
4 Uhore	1-1 S-Processor Line Plat 1-2 Merged XDP Connect	forms or for Processor and PCH			
ined	2-1 Intel® Flex Memory T	Technology Operations		23	}
	2-3 PCI Express* Related	on-Interleave (NIL) Modes Register Structures in the			
-	2-4 – Video Analytics Comr	non Use Cases			
2	2-6 Processor Display Arc	chitecture (with 3 DDI Port	s as an Example)	39	
-	2-7 DisplayPort* Overvie 2-8 HDMI* Overview	w			
	2-9 Example for PECI Hos	st-Clients Connection		46)
	2-10 Example for PECI EC 3-1 Device to Domain Ma	pping Structures			
		stemrastructure			
	4-1 Processor Power Stat	es		63	}
		nd IA Core C-States ent Breakdown of the Proc			
4	4-4 Package C-State Entr	y and Exit		71	age.
-	5-2 Thermal Test Vehicle	ol Thermal Profile for PCG 2	015D Processor	95	,
-		Thermal Profile for PCG 20 Thermal Profile for PCG 20			
defi.	5-5 Thermal Test Vehicle	Thermal Profile for PCG 2	015A Processor	98	}
dunce	5-6 Thermal Test Vehicle 7-1 Input Device Hystere	(TTV) Case Temperature sis	(TCASE) Measurement	Location 99) -
of inet.	9-1 Land Map (Top View,	Upper-Left Quadrant)		128	3
	9-2 Land Map (Top View, 9-3 Land Map (Top View,	Lower-Left Quadrant)		130)
Ġ	9-4 Land Map (Top View,	Lower-Right Quadrant)		131	defill
	define			ed	UII.
	dunce	inde,	¥	define	
	Inec	ined by		d uno	
unde		adefill		finec	
		ed ull.	nu ,		
Je,	def				
	4 nuo		indeli		46/11
	dinec		ed vi		nuc.
	unde	ade		fine	
		ed ull		unde	
rined br		4 und		uger.	
defill			ined o		
	unde		adefil.		1130
	9-3 Land Map (Top View, 9-4 Land Map (Top View,		ed un.		' nuge.
	inder	\(\)	efine		
Data	Input Device Hystere Joint Land Map (Top View, Joint Land Map (Top Vie	ined undefined u		inde ¹¹¹	L
Data	eti.,	istineu		rued ur	
ed une		, nuge,		adefil.	
efine			-61	11.	

undefined undefi I underfined underfine 2 undefined unde



		define and a sined a	ad un
		Processor Lines Terminology Related Documents Processor DRAM Support Matrix Supported DDR3L/-RS Non-ECC UDIMM Module Configurations (S-Processor Line) Supported DDR3L/-RS Non-ECC SODIMM Module Configurations (S-Processor Line)	18fines
		singo ed III.	
		der (Int	el
	9 n	, illipoo	
ight		ined a unit	
Inde	1-1	Processor Lines	11
roed or	1-2 1-3	Terminology	13
efil.	2-1	Processor DRAM Support Matrix	19
	2-2 2-3	Supported DDR3L/-RS Non-ECC UDIMM Module Configurations (S-Processor Line) Supported DDR3L/-RS Non-ECC SODIMM Module Configurations (S-Processor Line)	
	2-3	Supported DDR4 Non-ECC UDIMM Module Configurations (S-Processor Line)	
	2-5	Supported DDR4 Non-ECC SODIMM Module Configurations (S-Processor Line)	21
	2-6 2-7	DRAM System Memory Timing Support	
	2-8	PCI Express* Bifurcation and Lane Reversal Mapping	
464	2-9	PCI Express* Maximum Transfer Rates and Theoretical Bandwidth	28
, nuo		Hardware Accelerated Video Decoding	
ineo		Switchable/Hybrid Graphics Support	
efili	2-13	GT2 Graphics Frequency (S-Processor Line)	35
	2-14 2-15	VGA and embedded DisplayPort* (eDP*) Bifurcation Summary embedded DisplayPort* (eDP*)/DDI Ports Availability	36
	2-16	Display Technologies Support	37
		Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations	
		Processor Supported Audio Formats over HDMI* and DisplayPort* Display Resolution	
		S-Processor Line Display Resolution Configuration	
76		S-Processor Line Display Resolution Configuration when DP @ 30 Hz	
4 Union		HDCP Display supported Implications	
	2-24	Display Resolution and Link Rate Support	44
ger.		Display Bit Per Pixel (BPP) Support	
		Supported Resolutions1 for HBR2 (5.4Gbps) by Link Width	
	4-1	System States	64
	4-2 4-3	Processor IA Core/Package State Support	
	4-4	PCI Express* Link States	65
	4-5	Direct Media Interface (DMI) States	
	4-6 4-7	G, S, and C Interface State Combinations Deepest Package C-State Available	
ndefined und	4-8	Targeted Memory State Conditions	
Sine	5-1	Configurable TDP Modes	
	5-2 5-3	TDP Specifications (S-Processor Line)	
	5-4	Thermal Test Vehicle Thermal Profile for PCG 2015D Processor	95
	5-5	Thermal Test Vehicle Thermal Profile for PCG 2015C Processor	
	5-6 5-7	Thermal Test Vehicle Thermal Profile for PCG 2015B Processor	
	6-1	Signal Tables Terminology	100
		DDR3L/-RS Memory Interface	
100	6-4	DDR4 Memory InterfacePCI Express* Interface	102
sed u	6-5	DMI Interface Signals	104
defile	6-6 6-7	Reset and Miscellaneous Signalsembedded DisplayPort* Signals	105
undefined uni	6- <i>7</i> 6-8	Display Interface Signals	106
	6-9	Processor Clocking Signals	107
	6-10	Testability Signals	107
		Reset and Miscellaneous Signals	diner
Da	atasheet,	Volume 1 of 2	1
Da defined un	96 jiii	of the sed the	
-d ur		inde. Hefilia	
Gines		ined in	
		CITY AU	